# Abstract Proceeding of

# Micro2024

## 11th International Conference on

## Microelectronics, Circuits & Systems

## 16th and 17th May, 2024


Nanomaterial


Optoelectronic


Chip Febrication

## Organizer:

**Delhi Technological University, Delhi, India.**

## Co-organizer:

**Applied Computer Technology, Kolkata, West Bengal, India.**

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# Micro2024

11th international conference on

Microelectronics, Circuits and Systems

16th and 17th May, 2024

Vinod Dham Centre of Excellence for Semiconductors and

Microelectronics, Delhi Technological University, Bawana Road,

Shahbad Daulatpur, Rohini, Delhi-110042, India.



Proceedings Book with abstract of papers

Published dates: 16th May, 2024

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53 Teachers' Colony, Agarpara, Kolkata-700109, India

Inaugural Song:

**Prayer**
Translated in English
By
Hillol Ray
http://www.iwvpa.net/rayh
http://www.iwvpa.net/rayh/index-hra.php
Desires are all yours,
You are the universal star-
You do your own works, mom,
People say, I do them from a far!!

You stuck elephant into clay,
And push a handicap to ascend hill-
To some, you offer "Brahmo" feet,
And make others descend downhill!!

I am a machine, you are the machinist,
I am the home; you are the homemaker-

I am the chariot, you are the charioteer,
You drive as you like, and I am a happy taker!!

"Milestone"
June 25, 2019
Garland, Texas, USA

दिल्ली प्रौद्योगिकी विश्वविद्यालय
**DELHI TECHNOLOGICAL UNIVERSITY**
(Formerly Delhi College of Engineering)

विकसित भारत अभियान 1947 TO 2047

Prof. Prateek Sharma
Vice-Chancellor

**Message from the Vice-Chancellor**

Delhi Technological University (DTU), one of the top technological institutions in India, is consistently focusing on the research and development. All stakeholders of DTU are engaged in various path breaking innovative research activities. The conferences and seminars are frequently organized by the departments of DTU on contemporary and relevant topics in order to facilitate research in those areas which will lead to necessary metamorphosis in the academia as well.

The Vinod Dham Centre of Excellence for Semiconductors and Microelectronics at Delhi Technological University has been active in research and innovation and has setup an ambient academic environment for its researchers. With the commitment of highly qualified and efficient faculty, the Vinod Dham Centre of Excellence for Semiconductors and Microelectronics endeavours vigorously to make a mark in the field of research and development. The centre in association with Applied Computer Technology, Kolkata is organizing an International Conference on Microelectronics Circuits and Systems (MICRO-2024), during 16th-17th May, 2024, which is another venture to provide a platform for academicians - teachers, students, research scholars, and industry personnel - globally to discuss on contemporary trends and innovations in the field of science and technology.

On behalf of DTU, I welcome all participants of the Conference and wish them a happy stay at DTU and look forward for your participation in various events in the campus. Best wishes to MICRO-2024 and urge all participants to brainstorm on the various thrust areas of the conference.

(Prof. Prateek Sharma)

**SHAHBAD DAULATPUR, BAWANA ROAD, DELHI-110042, INDIA**
**PH.: 011-27882284, 27852207 Email: vedtu@dtu.ac.in, WEBSITE: www.dtu.ac.in**

# Editorial

These abstract Proceedings contain only the abstract of all registered papers of the conference, Micro2024. Some pages contain summary of talks of the invited Speakers, Keynote Speakers and some pages contain biodata of the speakers of this conference. Names, Photos and affiliations of all Speakers are available at end of this Proceedings.

About 85 papers are received and 50 are selected for presentations. Most of the papers are in the areas of Microelectronics, Circuits, Systems, MEMS, design and development of circuits, soft computing and optimization techniques, memory devices, storage circuits and devices. Some papers are on Nano-structures and Nanomaterials, Silicon and III-V Technology, CMOS scaling Issues, Sensor and IoT Networks, Analog/ RF and digital Circuits, VLSI, Power Electronics, Solid-state lighting, Optical Switch, Bio and Medical Electronics, Antenna Design etc.

Some good papers of this conference will be invited to forward to a special issue of the Journal of Microsystem Technologies of Springer-Nature, SCI indexed having impact factor=2.1. Some other papers are planned to be invited for possible inclusion to the Proceedings of LNEE (Lecture Notes on Electrical Engineering) book series of Springer having SCOPUS indexed and impact factor=0.6.

With due thanks and best wishes to all our team members including the Chief Guest, Keynote Speakers, invited speakers, chair persons, authors, participants etc. for sparing their valuable time in making the event a success in this typical pandemic period.

Papers of these abstract proceedings should not be referred as published papers but authors can mention that a paper is presented in the conference. After completion of the conference, most of these papers will be invited for online publications either for SCIE Journal or for SCOPUS Proceedings/book chapters. So, authors should not mention within any documents/biodata as online that this paper is published. Conference organizers may upload this abstract Proceedings in their website and allow downloading by free of cost. This should not be considered as publications by any plagiarism checking authority. This point should be kept in mind that for publication of a paper to any Journal, abstract publications has no problems.

The Editors
Micro2024

# Index

Invited Speaker

**Dr. Jacopo Iannacci,**

Centre for Materials and Microsystems (CMM),
Fondazione Bruno Kessler (FBK), Trento, Italy.

## Title of Talk:

## Píospccts of Micío/Na→ıo tcck→ıologics i→ı tkc GG scc→ıaíio witk focus o→ı RÏ-MEMS

## Abstract:

Looking at 2030 and ahead, 6G and Future Networks (FN) will relentlessly increase the variety of services on the move and provide immersive experience to end-users. After identifying and putting together performance trends and technology constraints already ongoing today with 5G, this contribution states that the well-established currently in use approaches to design and develop Hardware-Software (HW-SW) systems, are inappropriate to meet the challenges of 6G/FN. In response, a fresh concept of SW-mimicking HW is formulated here. The novel HW definition embodies features typically implemented by more complex HW-SW sub-systems, like, e.g., self-management, and it is forecasted to be crucial to empower 6G/FN, especially at the network edge. Microtechnology's and Nanotechnologies are identified as pivotal to this target.

Given such a frame of reference, the contribution focuses on RF-MEMS technology as an enabling tile in the identified complex scenario. To this end, recent advances at design and fabrication level are reported, with particular reference to key passive components, like micro-switches, reconfigurable step attenuators and multi-state phase shifters.

Invited Speaker


## Prof. Abhijit Biswas

Professor, Department of Radio Physics & Electronics, University of Calcutta, Kolkata, West Bengal, India. And General Chair (Publication, Micro2024).


### Title of Talk:

### The Dazzling Potential of Perovskite Solar Cells


**Abstract:**

Perovskite solar cells have garnered significant attention in the field of photovoltaics owing to their outstanding properties like tunable band gap and high absorption coefficient in the visible spectrum and promising advantages over traditional silicon-based solar cells. Their remarkable light-absorption capabilities, low-cost fabrication methods, and potential for high power conversion efficiency (PCE) make them a compelling candidate for next-generation solar energy technologies. The structure of perovskite solar cells typically consists of a layered configuration, with a perovskite absorber layer inserted between charge transport layers- Electron Transport Layer (ETL) and Hole Transport Layer (HTL).

This structure facilitates efficient photon absorption and charge carrier generation within the perovskite layer, while the adjacent transport layers enable the extraction and transport of generated carriers to the electrodes, resulting in direct generation of electricity.

Fabrication of perovskite solar cells involves a couple of process steps, including solution processing, layer deposition, and thermal treatment. Solution-based techniques such as spin-coating or inkjet printing are commonly utilized to deposit the perovskite layer onto a substrate, followed by deposition of charge transport layers using methods such as vacuum evaporation or chemical vapor deposition. Thermal annealing is then employed to improve the crystallinity and morphology of the perovskite film, optimizing its photovoltaic performance.

Recent reports in the field of perovskite solar cells have highlighted significant advancements in power conversion efficiency, stability, and scalability. Efforts to improve device stability through compositional engineering and interface engineering have led to enhanced long-term performance and reliability. Analytical models play a crucial role in understanding the fundamental mechanisms governing the operation of perovskite solar cells. We present here an accurate model for the calculation of photo generated current density based on materials and semiconductor physics, device physics, and optical properties and it is employed to optimize PCE of 2D Ruddlesden –Popper perovskite solar cells for two different architectures-nip and pin- together with various absorbing layer thickness and diverse ETLs and HTLs. Such a model provides valuable insights on the impact of charge carrier dynamics, recombination processes, and light absorption phenomenon on current- voltage characteristics of solar cells.

Looking ahead, the future scope of perovskite solar cells is promising, with ongoing research focused on further improving power conversion efficiency, stability, and reliability. Integration of perovskite solar cells into tandem solar cell architectures and building-integrated photovoltaics holds great potential for advancing the commercial applications of this emerging technology, paving the way for a sustainable green energy future.

Keynote Speaker


# Prof. Abhinav Kranti

Professor, Department of Electrical Engineering, Indian Institute of Technology, Indore, Madhya Pradesh, India


## Title of Presentation:

## Effectiveness of TCAD in Comprehending Unusual Characteristics of Junctionless Transistor


## Abstract:

The last few decades have witnessed the evolution of several MOSFET architectures. While each device has its advantages and challenges, it is imperative to comprehend the conduction mechanism associated with an evolving device. This is essential from the perspective of benchmarking the performance of an innovative device with respect to existing architectures. One such innovative architecture is the junctionless transistor which is able to showcase nMOS and pMOS functionality despite the absence of junctions. Apart from exhibiting characteristics similar to MOSFETs, the junctionless device has exhibited 'peculiar' effects such as sharp increase in drain with a subthreshold swing less than Boltzmann limit at room temperature and latching to the on-state during the reverse voltage sweep. These effects seem contrary to the 'known concepts' as the semiconductor region in a junctionless device is heavily doped with only one type of dopants. In addition, heavy doping in a confined region can lead to quantum effects which can influence the performance of nanoscale devices and circuits. The unusual phenomenon occurring in a junctionless transistor can be better understood through Technology Computer Aided Design (TCAD) tools which help in comprehending performance metrics not available through electrical characterization. The talk focuses on effectively utilizing TCAD tools for improved understanding and optimization of peculiar effects and quantum confinement in a heavily doped junctionless transistor. The application of unconventional features of junctionless transistors for application specific device design are also discussed.

Invited Speaker

**Prof. Mridula C Gupta,**

Professor, Department of Electronic Science, University of Delhi, South Campus, South Moti Bagh, New Delhi, Delhi, India - 110007

**Title of Presentation:**

**Phototransistor: An Innovation to Highly Sensitive and Energy Efficient Photodetector**

## Abstract:

Photodetectors (PDs) are semiconductor devices that convert optical energy into electrical energy and have gained considerable research interest due to their applicability to a wide range of applications, such as imaging, remote control, sensing, military applications, biomedical applications, optical communication, and environmental monitoring. Silicon-based PDs have been more attractive due to their low cost and monolithic integration with CMOS technology. Conventional Silicon-based PDs achieve maximum responsivity for wavelengths shorter than 1.1 μm due to the bandgap value of 1.1 eV of Silicon material, restricting its effective operation in the visible regime only. Thus, to select a particular spectrum of operation, different materials have been explored and reported in the literature with architectural advancements, including p-n photodiode, p-i-n photodiodes, avalanche photodiodes, Schottky photodiodes, MSM photodetector, heterostructures photodetectors, and phototransistors. Among these architectures, Field Effect Transistor (FET) based phototransistors have been proven very effective due to the low dark current and intrinsic high gain.

In FET-based photodetector using conventional designs, which illuminates the FET channel directly, the photo-excited carriers are generated in the channel, and the diffusion of these carriers limits the speed of the device. Thus, efforts have been made to separate the photo absorber material and the conduction material to overcome the speed limitation of phototransistors. Considering these facts, this work is based on photo absorber-gated metal oxide semiconductor field effect phototransistor. Here, the complete channel is covered with the thick photo absorber material between the gate and the gate oxide. The photo absorber material is chosen according to the wavelength of interest, where an optical voltage is generated inside it that controls the transistor conduction. The conduction occurs under the influence of optically generated voltage and applied biases. The modelling and simulation-based study of the phototransistor has been shown to optimize the best response for infrared and ultraviolet radiations. Along with the conventional MOSFET architecture, conventional tunnel field effect phototransistor and novel face tunnel field effect phototransistor has been shown with best optimized results obtained in the UV and the infrared region. Various optical Figure of Merits (FoMs) has been calculated to evaluate the performance of the phototransistors including sensitivity, responsivity, detectivity and response time. Finally, a summary of major findings for photo absorber gated field effect phototransistors has been presented for different architectures that proves its efficacy for better photodetector than conventional devices.

Invited Speaker

**Prof. Mukul Sarkar**

Professor, Department of Electrical Engineering, Indian Institute of Technology, Delhi, India.

## Title of Presentation:

## High Dynamic Range CMOS image sensors for automotives

## Abstract:

Automotives are no more just a mode of transportation, rather they have become sources of entertainment and information hubs. As the functionality inside the cars increases, a support system is also required for safety purposes. Image sensors have become an essential component in the current generation vehicles, enabling advanced driver assistance systems and autonomous driving features. These advanced functionalities have made driving safer, easier, and more comfortable. The number of automotive image sensors being used inside and outside a vehicle is growing at a rapid pace and is showing no signs of slowing down. These are primarily due to technological applications as well as legal mandates around the globe.

For safety drive assistance, automatic control, high data quality, and reliability of the acquired image are required. The lightning conditions in which the vehicle is being driven changes many orders of magnitude and therefore, the image sensors require to have a very high dynamic range. Dynamic range is defined as the the ratio between the highest brightness a camera can capture (saturation) and the lowest brightness it can capture. In this talk we will discuss the need for high dynamic range imaging sensors for automotive applications. Further, we will review the state-of-the-art imaging sensors providing HDR images.

Invited Speaker

**Dr Hab. Eng. Piotr Bojarczak**
Professor, Faculty of Transport, Electrical Engineering and Computer Sciences, URad Casimir Pulaski University of Radom, POLAND.

**Title of Presentation:**

**Application of deep learning methods in railroad track vision diagnostics**

**Abstract:**

The presentation will cover selected deep-learning topics about railroad track vision diagnostics. Two types of neural networks will be presented: shallow neural networks and deep neural networks. The main differences between the above-mentioned types of networks with emphasis on deep networks will be presented. Two types of deep networks for detecting the state of railroad track objects, traditional Yolo (You Only Look Once) networks and networks using language models - DETR (End to End detection with Transformer) will be presented. Next, the main areas of application of the above-mentioned networks in rail transportation will be presented. These will include visual diagnostics of railroad track conditions (state of sleepers, rail fastenings to sleepers, turnouts) and the types of rail defects. The second area of application is the detection of dangerous events involving humans or animals that occur along the railroad track or at level crossings. The third area of application is the use of networks for the detection of fixed railroad infrastructure elements such as semaphores, and turnouts. Finally, the issue related to the problem of limited learning data occurring in deep learning networks and ways to reduce its number by using data augmentation and transfer learning will be presented.

Invited Speaker

**Dr. Ashwini K Aggarwal**
Director, Applied Materials India Pvt. Ltd.,
Faridabad, Haryana, India.

**Title of presentation:**

**Materials Engineering for Semiconductors/ Advanced Packaging**

**Abstract:**

As industry looks at optimizing on PPACT (power, Performance, Area, Cost and Time-to-market), materials engineering is playing a decisive role in driving the new chapter of technology evolution in emerging sectors. Advanced Semiconductor Packaging is gaining momentum as the dies transit to lower geometries and chiplet engineering becomes the buzzword. The key drivers in the new paradigm are the market driven pressures of lower cost per i/o as the # of i/o scale per chip – as well as increased functionality in demanding geometries and applications. The talk will introduce the audience to the panel-level packaging and engineering solutions from Applied Materials.

Invited Speaker

**Dr. Mukesh Jewariya**
Senior Scientist, National Physical laboratory,
CSIR (Council of Scientific and Industrial Research), Delhi, India.

**Title of Presentation:**

## Terahertz Computed Tomography and its Prospectus

**Abstract:**

A novel technique has been demonstrated for the generation of intense terahertz electromagnetic wave that enables high-field near-single-cycle terahertz (THz) pulse via non-collinear $\chi$ (2) process in LiNbO 3 with both phase-front and spectral angular dispersion. Using this technique we are able to generate a single cycle (broadband) terahertz pulse upto an electric field of 750kV/cm We have also demonstrated the potential of this intense THz pulse for 3D THz imaging, which is 13- times higher than that of previous system based on collinear optical rectification in ZnTe crystal. The main advantage of the proposed method relies on real-time THz line projection providing 10 ms acquisition time of 2D-ST THz image. Therefore, 3D THz CT has been performed in only 6 minutes, representing a significant improvement compared with common systems. Finally, demonstration of 3D images clearly indicated a high potential for sensing, non-destructive inspection and material characterization in real world applications.

Keynote Speaker

## Dr. Meena Mishra

Director, Solid State Physics Laboratory (SSPL), DRDO, Delhi, India.

### Biography:

Dr. Meena Mishra is the Director of the Solid-State Physics Laboratory (SSPL), which is part of the Defense Research and Development Organisation (DRDO) in Delhi, India. Her Position: Director, Solid State Physics Laboratory (SSPL), DRDO. Her Education: Master of Science in Electronics from Delhi University, India (1986) and Doctor of Science from Jamia Millia Islamia University, India (2005). Her Career: Joined Solid State Physics Lab as Scientist B in 1989 Progressed through various roles to Scientist E, Appointed as Director of SSPL in 2023 Her Research: She has over 26 years of experience in the area of MMIC design and RF Characterization. She has been involved in the division responsible for RF Characterization, Device modelling, MMIC, and Module design of GaN HEMT based technology. The Solid-State Physics Laboratory (SSPL) under her leadership is engaged in the research and development of advanced semiconductor materials and devices. The lab has developed several solid-state devices like Gunn, Schottky Barrier, and IMPATT Diodes, among others. For more detailed information, you may refer to the official DRDO website or other scientific publications where her work is cited.

Invited Speaker

## Dr. Jacopo Iannacci,

Centre for Materials and Microsystems (CMM), Fondazione Bruno Kessler (FBK), Trento, Italy.

### Biography:

Jacopo Iannacci (Senior Member, IEEE) was born in Bologna, Italy, in 1977. He received the M.Sc. (Laurea) degree in electronics engineering from the University of Bologna, Bologna, in 2003, and the Ph.D. degree in information and telecommunications technology from the Advanced Research Center on Electronic Systems "Ercole De Castro" (ARCES), University of Bologna, in 2007.,He received the Habilitation as an Associate Professor in electronics from the Italian Ministry of Education, University and Research (MIUR), Rome, in 2017 and the Habilitation as a Full Professor in electronics from the Italian Ministry of University and Research (MUR) in 2021. From 2005 to 2006, he worked as a Visiting Researcher at the DIMES Technology Center (currently Else Kooi Laboratory), Technical University of Delft, Delft, The Netherlands, focusing on the development of innovative packaging and integration technology solutions for radio frequency passives in micro-electromechanical system (MEMS) technology (RF-MEMS). In 2016, he visited as a Seconded Researcher at the Fraunhofer Institute for Reliability and Micro Integration IZM, Berlin, Germany, to conduct high-frequency characterization of RF-MEMS components jointly with the RF and Smart Sensor Systems Department. Since 2007, he has been a Researcher (permanent staff) at the Center for Sensors and Devices, Fondazione Bruno Kessler, Trento, Italy. He has authored more than 130 scientific contributions, including international journal articles, conference proceedings, books, book chapters, and one patent. His research interests and experience fall in the areas of finite-element method (FEM) Multiphysics modelling, compact (analytical) modelling, design, optimization, integration, packaging, experimental characterization, and testing for reliability of MEMS and RF-MEMS devices and networks for sensors and actuators, energy harvesting (EH-MEMS) and telecommunication systems, with applications in the fields of 5G, the Internet of Things (IoT), future 6G, tactile Internet (TI), and super-IoT. Dr. Iannacci has been a member of the Editorial Board of Microsystem Technologies (Springer) since 2015. He is currently an Associate Editor of Microsystem Technologies (Springer) and Frontiers in Mechanical Engineering. He is involved in several international conferences as the Symposium Chair/Co-Chair, the Session Chair, a Technical Program Committee Member, an International Advisory Board Member, a Tutorial Lecturer, and an Invited Speaker, among which the following few are mentioned: IEEE Sensors Journal; IEEE 5G World Forum (5GWF)/Future Networks World Forum (FNWF); Society of Photo-Optical Instrumentation Engineers (SPIE) Micro Technologies; European Solid-State Circuits Conference / European Solid-State Device Research Conference (ESSCIRC-ESSDERC).

Keynote Speaker:

## Prof. M. Jamal Deen,

Distinguished University Professor, Director, Micro- and Nano-Systems Laboratory, Electrical and Computer Engineering Department, School of Biomedical Engineering, McMaster University, 1280 Main Street West Hamilton, ON L8S 4K1, CANADA,

### Biography:

Prof. M. Jamal Deen is a distinguished academic with a wealth of experience and contributions to the field of electrical engineering and applied physics.

- Current Positions: Distinguished University Professor, Senior Canada Research Chair in Information Technology, Director of the Micro- and Nano-Systems Laboratory (MNSL)
- Affiliations: Electrical and Computer Engineering Department, School of Biomedical Engineering, McMaster University
- Education:
  - Ph.D. in Electrical Engineering and Applied Physics, Case Western Reserve University, Cleveland, Ohio, USA (January 1986)
  - M.S., Case Western Reserve University, Cleveland, Ohio, USA (May 1982)
  - B.Sc., University of Guyana, Guyana, South America (1978)
- Awards and Honors: Prof. Deen has received numerous awards and holds several fellowships, including FRSC, FCAE, FIEEE, and many others.
- Research Interests: His research spans across micro-/nano-/opto-electronics, nanotechnology, and data analytics with applications in health and environmental sciences.

Invited Speaker

## Prof. Abhijit Biswas

Professor, Department of Radio Physics & Electronics, University of Calcutta, Kolkata, West Bengal, India. And General Chair (Publication, Micro2024).

### Biography:

Abhijit Biswas holds B.Tech., M.Tech., and Ph. D. (Tech.) degrees from the University of Calcutta. He joined the University of Calcutta in 1999 as a Lecturer, worked as the Head of the Department during 2020-2022, and currently serves as a Professor in the Department of Radio Physics and Electronics. He was associated with Jadavpur University as a Reader in the Department of Electronics and Telecommunication Engineering during 2006–2008. In the meanwhile, he worked at Interuniversity Microelectronic Center (IMEC), Belgium in 2007. Dr. Biswas specializes in semiconductor physics, electronic and optoelectronic devices, optical communications, and photovoltaics. He has an extensive publication record, with 87 papers in International SCI Journals and over 150 papers in International Conference Proceedings. Notably, he already supervised 12 Ph. D. scholars, and is currently supervising 6 Ph. D. scholars. He conducted many government-funded research projects including SERB and CSIR. He has also contributed as a Guest Editor for Microsystem Technologies, Springer, and as a reviewer for prestigious journals including IEEE Electron Device Letters, IEEE Transactions on Electron Devices, IEEE Transactions on Nanotechnology and Optical Materials. Dr. Biswas was acknowledged for his contributions, receiving the UGC research award from 2012 to 2014. In August 2019, he was further honored with the "Best Citizen of India Gold Medal Award" for his exceptional service to academia and society.

Keynote Speaker

## Prof. Abhinav Kranti

Professor, Department of Electrical Engineering, Indian Institute of Technology, Indore, Madhya Pradesh, India

### Biography:

Prof. Abhinav Kranti is a distinguished faculty member in the Department of Electrical Engineering at the Indian Institute of Technology (IIT) Indore, Madhya Pradesh, India.

- **Affiliation**: Department of Electrical Engineering, IIT Indore
- **Research Interests**: Prof. Kranti's research spans several areas including:
  - Solid-State Devices
  - Circuit Design
  - Nanotechnology
  - Low power circuit design with nanoscale devices
  - Design and analysis of GaN and ZnO based HEMTs1

He leads the Low Power Nanoelectronics Research Group, which is engaged in pioneering research on:

- Capacitorless dynamic random-access memory (DRAM)
- Steep switching devices
- Material-device-circuit co-design
- Vertically stacked transistors

Invited Speaker

## Prof. Mridula C Gupta,

Professor, Department of Electronic Science, University of Delhi, South Campus, South Moti Bagh, New Delhi, Delhi, India - 110007

### Biography:

Prof. Mridula C Gupta is a Senior Professor and Head of the Department of Electronic Science at the University of Delhi, South Campus. Her educational qualifications are quite impressive, with a Ph.D. in 1998, an M.Tech. in 1988, an M.Sc. (Electronics) in 1986, and a B.Sc. (Hons.) (Physics) in 1984, all from the University of Delhi. Her career profile includes various roles at the Department of Electronic Science, University of Delhi, where she has been contributing since 1989. She has also held administrative positions such as Joint Dean Examination and Joint Dean Student Welfare at the University of Delhi. For a detailed biodata, including her publications, research interests, and administrative assignments, you can refer to her profile on the University of Delhi's official website.

Invited Speaker

## Dr. Moumita Mukherjee

Professor and Dean (R & D), Adamas University, Barasat, Kolkata, West Bengal, India.
(Ex. Sr. Scientist of DRDO Centre of Excellence) (under Ministry of Defence, Govt. of India).

**Biography:**

Dr. Moumita Mukherjee is alumni of R K S M Sister Nivedita Girls' School - Kolkata, Presidency College and Calcutta University. She received M.Sc. (Physics) with specialization in Electronics & Communication, M.Tech. in Biomedical-Engineering and Ph.D. (Tech.) in Radio-Physics and Electronics (2009), University of Calcutta, India. She did her doctoral & post-doctoral studies under DRDO, Ministry of Defence, Govt. of India. She received 'visiting scientist' & 'postdoc' positions from INEX, Newcastle University, UK & Technical University, Darmstadt, Germany. Dr. Mukherjee was attached with DRDO Centre under Ministry of Defence, Govt. of India (2009-2015) as Scientist (Reader grade). In continuation to that she joined Adamas University and presently working as Professor – Dept. of Physics & Dean (R&D) after completing her terms as Associate Dean & Academic coordinator (2016-2020), Associate Professor (2017-2020) & Assistant Professor III (2015-2017), in the same University. With a total seventeen years of R&D and teaching experience, she is Visiting / Adjunct Professor of JAP-BMI under Calcutta University and the West Bengal University of Health Sciences. She is empaneled examiner, moderator and PhD supervisor under public & private Universities in West Bengal. She has guided more than 35 Post-Graduate thesis & 12 Ph.D. theses as Supervisor/Jt. Supervisor. Her research interest is focused on THz-electronics, Semiconductor devices, Graphene electronics, Photo-sensors, nano-biosensors and Medical Electronics & instruments. She has published more than 150 peer-reviewed research papers, till date, in reputed international refereed journals and reviewed proceedings with citation globally (citation: 900+, h-index: 16). She is principal investigator of 7 (Seven) Government of India (DRDO) & start-up /industry funded research projects of ~111.30 Lakhs worth.

Invited Speaker

## Prof. Mukul Sarkar

Professor, Department of Electrical Engineering, Indian Institute of Technology, Delhi, India.

**Biography:**

Mukul Sarkar received his M.Sc degree in Biomedical Engineering from University of Technology, Aachen, Germany in 2006 and Ph.D. degree in Electronic Instrumentation Engineering from the Technical University of Delft, The Netherlands in 2011. He was a full-time resident of IMEC from 2007 to 2011 during his Ph.D. After his Ph.D he spent a year as postdoctoral researcher with Electronic Instrumentation Laboratory, Technical University of Delft, The Netherlands. Between 2003 and 2005, he worked in the Philips Institute of medical information, Aachen, Germany as a research assistant in detection and analysis of bio-signals. Since February 2012 he is with the department of Electrical Engineering at Indian Institute of Technology, Delhi, where currently he is an Associate Professor. His research interests lie in the areas of solid-state imaging, CMOS Image sensors, Bio-inspired vision systems, Analog/Digital circuit design, Optoelectronics and Machine vision.

Invited Speaker

## Dr Hab. Eng. Piotr Bojarczak

Professor, Faculty of Transport, Electrical Engineering and Computer Sciences, URad Casimir Pulaski University of Radom, POLAND.

### Biography:

Hab. Dr. Eng. Piotr Bojarczak is working as a professor in the Faculty of Transport, Electrical Engineering and Computer Science at Casimir Pulaski Radom University, Poland. He graduated Doctor of Philosophy (Ph.D.) in Electrical Engineering from Warsaw University of Technology. His research areas include image processing, neural networks, deep learning, and the application of AI in the diagnostics of railway infrastructure. He has about 50 scientific publications. He has experience of working in industries like Graw, Infracert, Telesto, Signalling, and Telecommunications Department of Polish Railway Lines.

Invited Speaker

## Dr. Ashwini K Aggarwal

Director, Applied Materials India Pvt. Ltd., Faridabad, Haryana, India.

### Biography:

Dr. Ashwini K Aggarwal has a notable academic and professional background. Here's a brief biodata based on the available information:

- **Educational Qualifications:**
  - **B.Tech.** in Textile Technology from **IIT Delhi** (1986), graduated with a silver medal1.
  - **M.S.** and **Ph.D.** in Chemical Engineering from the **University of Rochester**, New York, USA (1992).
- **Professional Experience:**
  - Currently the **Director** at **Applied Materials India Pvt. Ltd.**, Faridabad, Haryana, India.
  - Previously a **Professor** at the Department of Textile Technology, **Indian Institute of Technology (IIT) Delhi**.
- **Research Interests:**
  - Smart and intelligent textile materials.
  - Nanomaterials.
  - Plasma processing.
  - Fiber manufacturing.
- **Specializations:**
  - Developing new fibers from organic and inorganic materials for new applications. Production of nanofibers using electrospinning and development of Nano finishes based on nanoparticles.
  - Microencapsulation process for organic and inorganic phase change materials (PCMs) and development of new inorganic PCMs. Processing of textile and other materials using indigenous atmospheric pressure glow discharge.

Invited Speaker

**Dr. Mukesh Jewariya**

Senior Scientist, National Physical laboratory,
CSIR (Council of Scientific and Industrial Research), Delhi, India.

Dr. Mukesh Jewariya received the M.Sc. in physics in 2003 from Indian Institute of Technology Roorkee and M.Tech. in laser technology in 2006 from Devi Ahilya Vishwavidyalaya Indore. He received his D.Sc. in physics from Kyoto University in 2010. From 2010 to 2011, he worked as a Specially Appointed Researcher in the Renovation Center of Instruments for Science Education and Technology, Osaka University. Later from 2011-2012 he worked as an Assistant Professor in the Institute of Technology and Science, The University of Tokushima, Tokushima, Japan. He was a visiting scientist from 2015- 2017 at Korea atomic Energy Research Institute-Daejeon, S. Korea. Currently he is working as a Senior Scientist at CSIR-National Physical laboratory New-Delhi from 2012. He is a recipient of Monbukagashuo Fellowship- Japan (2006), JSPS Kakenhi (2011) and Korean Research Fellowship ( 2015-2017). Other than he is qualified GATE, CSIR NET, JEST. He has more than 53 publication, 2 book chapter and more than 60 conference papers. He is a life member of Indian Physics Association, Indian Laser Association, Optical Society of America, Optical Society of India, Japanese Physical Society, Korean Physics Society. He is an editorial board of Optical Materials, Optical Communication and other journals. He is reviewer of many journal including PRL, PRB, IEE, JOSA-A, JOSAB, Optical Letters – Materials-Express etc. His research interest includes generation of high power THz pulse, THz spectroscopy, THz imaging, and THz frequency metrology, Length Metrology, Dimensional Metrology, Development of Materials for Terahertz detectors and Ultrafast Spectroscopy. His current interest is to Realize SI unit Metre using Quantum standard (Optical Frequency Comb).

General Chair (Publications) and Vidyasagar Awardee

## Prof. Abhijit Biswas

Professor & HOD, Department of Radio Physics & Electronics, University of Calcutta, Kolkata, West Bengal, India. And General Chair (Publication, Micro2024).

### Biography:

Abhijit Biswas (M'12) received the M.Tech. and Ph.D. degrees from the Department of Radio Physics and Electronics (RPE), University of Calcutta, Kolkata, India. He is currently a Professor with the Department of RPE, University of Calcutta. *(Based on document published on 12 April 2016).*

The Lotfi A Zadeh Memorial Awardee

## Prof. R. S. Gupta

Professor, dept. of ECE, MAIT, Delhi, India.

### Biography:

Certainly! Here is the biodata of Prof. R. S. Gupta from the Department of Electronics and Communication Engineering at Maharaja Agrasen Institute of Technology (MAIT), Delhi, India:

- **Educational Qualifications**:
  - B.Sc. (Physics, Chemistry, Maths) - Agra University, 1963
  - M.Sc. Physics (Electronics) - Agra University, 1966
  - Ph.D. (Electronics Engineering) - Institute of Technology, Banaras Hindu University, 1970
- **Professional Memberships**:
  - Life Senior Member IEEE – SM 07132517
  - Life Fellow (LF) – The Institution of Electronics and Telecommunication Engineers – F-023099
  - Member – India Chapter ICTP (Italy)
  - Life Member – Semiconductor Society (India)
  - Chairman – Society for Microelectronics and VLSI
  - Chairman – IEEE-EDS Delhi Chapter (2007-2011)
  - Member IEEE EDS Delhi Chapter (2012-continued)
- **Teaching & Research Experience**:
  - Professor at MAIT since May 1, 2010
  - Emeritus Scientist (CSIR) at University of Delhi from May 2008 to May 2009
  - Professor at University of Delhi from Nov. 19, 1997 to Jan. 9, 2008
  - Lecturer in Reader grade at Ramjas College from Jan. 1, 1986 to Nov. 18, 1987
  - Lecturer at Ramjas College from Aug. 27, 1971 to Dec. 31, 1985
  - Part-time lecturer & research fellow at Institute of Technology Banaras Hindu University from Dec. 1, 1967 to Aug. 26, 1971
  - Lecturer at V.S.S.D. College, Kanpur from Aug. 1, 1967 to Nov. 30, 1967
  - Lecturer at S.K.K. College, Etawah from August 1966 to July 31, 1967
- **Research Specialization**: Solid State Electronics Devices, VLSI Design, and modeling of Microelectronic Devices (MOSFET, MESFET, HEMT)
- **Publications**: More than 650 publications in various international/national journals and conferences
- **Ph.D. Students Guided**: 39 students have obtained their Ph.D. degrees under his guidance, and he is currently supervising 6 students

Paper ID: 03

# Design and Implementation Of A Planar Uwb Antenna With Bandnotch Characteristics

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**Abstract**: A radiating metallic patch with a multiband and multi-rejection characteristic acts as the planar ultra wide band (UWB) system. The modelled structure working from 1 to 12 GHz achieved a wide band response or overall bandwidth of 5.1 GHz and a total notch band of 5.9 GHz. To attain the appropriate frequencies for the band-operation features, two long rectangular spiral strips are created on either side of the transmission line or feed line specified on the substrate and employed in the planar layout of the UWB model. The metallic patch integrates the meta-material complimentary split ring resonator CSRR, and the notched out frequency range is regulated by the size, slots, and circular cuts of the CSRR structure. The simulation and testing results of the fabricated model reaching S1,1 -10dB, VSWR 1.45, and Gain > 4dB for all operational frequencies verify the comprehensive accomplishment of the drafted antenna model. Multiband rejection at (2.24 to 2.84) GHz with a strong notch at 2.4GHz Bluetooth IEE802.11b, (3.215 to 4.695) GHz with a strong notch at 3.5GHz and 3.8GHz WiMax, (5.67 to 6.46) GHz with a strong notch at 6GHz WLAN, WIFI 6E, and (7.05 to 10.27) GHz with a strong notch at 8.9GHz, X Band applications

**Keywords:** (Multi Band rejection or notch, multi band operation, CSRR, rectangular spiral strips, UWB)

Paper ID: 04

# Smart Crop: Intelligent Crop Recommendation System using Machine Learning

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**Abstract:** Agricultural sector plays a pivotal role in global food security and economic stability. Maximizing crop yield and minimizing resource wastage is of paramount importance in this context. Crop recommendation systems (CRS) are important tools used by agronomists and farmers to optimize crop yield and improve food security. Recent advances in machine learning techniques, particularly ensemble learning, have made it possible to develop more accurate and efficient CRS models. This study introduces a new method of creating a CRS by combining a variety of machine learning methods, such as gradient boosting, Stacking Classifiers, random forests, and decision trees. The suggested system provides suggestions for crop selection and management by accounting for several variables, comprising soil quality, climatic patterns, and nutrient levels. The model's performance was assessed using an actual dataset and contrasted with other CRS models that were already in use. The findings show that the suggested system operates more accurately and efficiently than alternative models. Furthermore, the CRS is designed with a user-friendly interface, making it accessible to farmers, agronomists, and stakeholders in the agricultural domain. The system provides intuitive visualizations and explanations for the recommended crops, empowering users to make informed decisions based on the model's outputs. Overall, the study shows the potential of using machine learning with ensemble learning techniques in developing more effective and reliable CRS models.

**Keywords:** Crop Recommendation System, Machine Learning, Ensemble Learning, Precision Agriculture, Sustainable Agriculture, Agricultural Decision Support, Random Forest, Stacking Classifier, Gradient Boosting.

Paper ID: 06

## Analysis of LED bulb by mathematical and simulation methods with porous fin material with square-shaped extruded fins in passive cooling mode

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**Abstract:** LED bulbs dominate more than 90% of the lighting industry worldwide for lighting purposes. However, literature reviews indicate that LED bulbs face significant challenges in heat dissipation, which can affect their lifespan. For instance, a mere 1°C increase in temperature can reduce the bulb's life by 12,000-18,000 hours. Both active and passive cooling systems are commonly employed to address this issue. While active cooling systems are effective, they tend to be more expensive compared to passive alternatives. This paper focuses on the passive cooling system of a 50W street-light lamp. The analysis considers parameters such as density, kinematic viscosity, velocity, junction temperature, porosity, heat transfer rate, laminar flow, and heat transfer modes. The findings suggest that using square-shaped fins with a 1 mm diameter drill can enhance convection heat transfer, resulting in a 21.8% increase in surface area. Additionally, the "Plus" shape of the fins facilitates the formation of an air swirl, contributing to a 30.41% decrease in heat sink temperature. Furthermore, material porosity enhances cooling rates by generating swirls and promoting upward airflow. Ultimately, square-shaped fins emerge as an optimal solution for passive cooling systems, mimicking the efficiency of active cooling systems.

**Keywords:** Porosity; Heat transfer coefficient; laminar Flow; heat transfer rate by convection.

Paper ID: 08

## Single Event Upset Analysis of 12t Sram Cell for Deep Space Application

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**Abstract**: Technological progress has led to a swift reduction in transistor size and spacing between them. Consequently, the vulnerable nodes' essential charge has gone down, which makes SRAM cells less susceptible, widely utilized in deep space contexts, more prone to soft errors. When radiation particles impact a Every point in the typical 6T SRAM (short cell, it triggers a bit flip in the stored data, causing an upset to occur only once (the SEU). In response to this issue, we introduce an innovative approach in this study: the Soft-Error-recovery 12a pulse SRAM cell with minimal power consumption. The goal of this discovery is to reduce SEUs. Importantly, all sensitive nodes within the 12T design are equipped to restore their original data, even if a radiation-induced upset causes a change in node values. Additionally, 12T exhibits resilience against the impact at its associated nodes for archiving of single-event multi-node disruptions (SEMNUs). In essence, our proposed 12T SRAM cell offers a strategic solution to the growing vulnerability of SRAM cells to soft errors. Its durability against various types of upsets, coupled with its enhanced stability, power efficiency, and write performance, highlights its potential to propel advancements in deep and aerospace and related applications.

**Keywords:** Static noise margin (SNM), (SEU), (SEMNUs), access time, emission toughness, equilibrium between consuming literature, and cursive competencies.

Paper ID: 10

## Online Restaurant Table and Food Booking System

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Alamuri Ratnamala Institute of Engineering and Technology

**Abstract:** The focal point of the project is centered on the development of an Android application tailored for restaurant table and menu reservations. In the past, manual reservation systems prevailed, requiring customers to make reservations via phone calls or in-person visits. However, with the advent of digital solutions, there has been a notable shift towards more efficient and streamlined processes. The primary objective is to create a sophisticated system that not only enhances the overall dining experience but also significantly saves time and resources for both customers and restaurant staff alike.The proposed system introduces a seamless and convenient approach to reservation management, empowering customers to effortlessly book tables, menus, or both through the online platform. Moreover, to secure menu bookings, customers are required to make a 50% upfront payment, ensuring commitment and reducing the likelihood of no-shows. By embracing this digital reservation system, restaurants can optimize their operations, minimize errors, and enhance customer satisfaction. Ultimately, the implementation of such an innovative solution reflects a forward-thinking approach towards modernizing restaurant services and meeting the evolving needs of patrons in today's digital age.

**Keywords:** Android Application, Table Booking, Menu Booking.

Paper ID: 12

## OpenCV-based Virtual Interactive Board by Using Python

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Mayank Mangal
Department of Information Technology ARMIET, University of Mumbai, Maharashtra, India
Krishna Kamble, Samarth Jagakar, Samir Pawar, Siddharth Kamble
Department of Computer Science & Engineering-AIML, ARMIET, MU, Maharashtra, India

**Abstract:** The OpenCV-based virtual interactive board module provides the user interface with interactive whiteboards. As opposed to the traditional approaches to vocabulary
teaching and learning, much research has reported on using virtual whiteboards to enhance the way of teaching and improve the standard of teaching. Implementing the interactive board in the present education system will increase student-teacher interaction and the way of communication between them will get improved. An OpenCV-based virtual interactive board was an immense, virtual gesture-based application. The user can control the computer virtually by making hand gestures. Through this OpenCV library, we made various functions based on hand gestures and programmed them as required. We created this tool for Selecting colors, Eraser mode, Writing, and presentation mode. In the OpenCV-based virtual interactive board, by selecting writing mode and board type, users can write on the screen using different colors by just fingertip movements in the air and users can erase the board partially using the eraser option or completely by waving five fingers on the screen and by selecting presentation module the user enters into presentation module and there user can give presentation by moving slides fourth and back just by hand gesture in air and user can also write or markup.

**Keywords:** Interactive whiteboard; OpenCV; Computer Vision; Python.

Paper ID: 13

## QAM-DCNN: Design and Development of the Novel Secure Edge Framework for Effective Disease Prediction using Quad Attention Module deep CNN Classifier

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Department of Computer Engineering, Mumbai University, Maharashtra, India,

**Abstract:** This research article aims to develop a secure framework for the detection of disease in patients using edge based multi data acquisition and data processing. The gathered data will be stored in the cloud & access will be provided through a trapdoor. The decision maker module will aggregate and pre-process the data, and the Quad attention module based deep CNN classifier will predict the disease, which effectively reduces the computational complexity and predicts the disease of the patients. The predicted information will be shared to the patients through the cloud and the research is believed to achieve high performance than some of the existing methods.

**Keywords:** Healthcare; Deep CNN; Edge Computing.

Paper ID: 14

## CD-Deep LSTM: Effective Credit Card Fraud Detection Model based on Clustered Distributed based Deep LSTM Model.

Swati Jadhav, Vivek Pandey, Manoj Patil, Supriya Pawar
Department of Computer Engineering, Mumbai University, India,
Ravi Jeswani
Department of Mater of Management Studies, Mumbai University, India,

**Abstract:** In this research article is to purpose a distributed clustered LSTM model for CC fraud identification or detection. To optimize the model, many techniques are applied such as normalization, modified optimized clustering, grey coyote optimization, k-means clustering, and a bio-inspired CC (Credit card) fraud identification model based on user behavior analysis suitable for business management in electronic banking. The grey coyote optimization, which aids in adjusting the deep LSTM classifier's weights and bias and facilitates credit card identification, determines the study importance. Performance indicators including specificity, sensitivity, and accuracy will be contrasted with current techniques.

**Keywords:** Credit card (CC) fraud detection; Deep LSTM; Deep Learning

Paper ID: 16

# Exploring the impact of structural defects on propagation characteristics and properties of co-existing multiple topological interface states

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Somnath Ghosh
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**Abstract:** The junction of two topologically distinct lattices supports topological interface states which can exhibit highly stable, scattering-free and robust properties. We investigate the propagation characteristics and properties of the co- existing multiple topological interface states in a real- world multi-channel topological optical fiber associated with structural defects and deformation in shape. The tolerance analysis in the presence of deliberate structural imperfections below 4% with reference to the annular area at the topological junction of trivial and non-trivial lattice show both propagation characteristics and robustness properties of multiple topological interface states remain intact, unaffected even by a deliberate structural deformation resulting in an asymmetrical elliptic topological junction featuring major-to-minor axes ratio below 1.1. The obtained results suggest that there is no significant change in propagation characteristics and properties of the co-existing multiple topological interface states when the structural defects and junction deformation remain within a certain limit as opposed to the state-of-art conventional optical fibers which remain highly sensitive to any form of structural imperfections and/or defects leading to the loss of information/data during transmission. Therefore, indicating that topological optical fiber systems could outperform conventional optical fibers in achieving structural defect immunity during transmission.

**Keywords:** Mid-infrared, propagation characteristics, topological interface states, topological optical fiber, Zak phase

Paper ID: 19

## Design and analysis of eco-friendly all-inorganic 2D/3D multi-junction perovskite tandem solar cell with an efficiency of 28.15%

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**Abstract:** Multi-junction tandem solar cells are a promising photovoltaic device for achieving high-efficiency solar energy conversion. In this work, we leverage device simulation techniques to thoroughly investigate the performance characteristics of a novel lead-free all- inorganic all-perovskite tandem solar cell configuration. Our proposed device incorporates a two-dimensional perovskite absorber in the top cell (ITO/WS2/Cs3Bi2I9/Cu2O) and a three-dimensional perovskite absorber in the bottom cell (WS2/RbGeI3/Cu2O/Au). This design strategy is meticulously tailored to ensure optimal light absorption across the visible solar spectrum. By utilizing a standard AM 1.5G spectrum and a filtered spectrum for the top and bottom cells, respectively, coupled with thickness optimization to achieve current matching conditions, we propose a champion tandem structure. Notably, our champion tandem cell, featuring top and bottom cell thicknesses of 900 nm and 263 nm, respectively, exhibits improved performance metrics: an open-circuit voltage (VOC) of 2.22 V, a short-circuit current density (JSC) of 14.30 mA/cm2 , a fill factor (FF) of 88.67%, and a power conversion efficiency (PCE) of 28.15%.The obtained results indicate a significant advancement in enhancing the efficiency of eco-friendly perovskite solar cells.

**Keywords:** All-perovskite tandem solar cell, lead-free perovskite solar cell, multi-junction solar cell, 2D/3D tandem solar cell.

Paper ID: 26

## A study on PKL alternating current (AC) generation for practical utilization using green synthesized of silver nanoparticles (AgNPs)

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Department of Physics, Jahangirnagar University, Savar, Dhaka
K. A. Khan
Department of Physics, Jagannath University, Dhaka-1100

**Abstract:** A study for DC load voltage, AC load voltage, internal resistance, maximum power, open circuit voltage and short circuit current have been measured for practical utilizations. An inverter has been used to convert DC electricity in to AC electricity. The variation of DC load voltage and the variation of AC load voltage with time have been studied. It is seen that for without AgNPs the change of AC load voltage is greater than the change of DC load voltage. It is also seen that for without AgNPs the change of AC load voltage is greater than the change of DC load voltage. But the it is also seen that for with and without AgNPs the change of both DC and AC load voltages are greater than the change of both DC and AC load voltages respectively. It is also found that the internal was reasonable for 160 hrs time duration. The maximum internal resistance was 3.43 ohm and the minimum internal resistance was 3.31 ohm without use of AgNPs. The difference was 0.12 ohm. It has been synthesized AgNPs using PKL extract. The effect of AgNPs have studied for use in both DC and AC appliances. It is shown that the performances of AgNPs are better for both DC and AC appliances.

**Keywords:** Alternating current, AgNPs, AC load voltage, DC load voltage, Green synthesis, Direct current, PKL electrochemical cell

Paper ID: 28

## Full Adder Design Utilizing GDI Technique for Energy-Efficient Arithmetic Operations

V V Satyanarayana Satti, Purna Venkata Satya Aditya Raja, Thamarai M, Sudheer Reddy S, Sabari Manikanta K and Ganesh V
Department of Electronics and Communication Engineering, Sri Vasavi Engineering College, Pedatadepalli, Tpg, 534101, AP, India.

**Abstract:** In recent years, there has been a growing demand for energy-efficient computing solutions, driven by the rise in portable devices, IoT applications, and data center. The full adder, a fundamental arithmetic block utilized in computing, signals processing, and image processing, plays a pivotal role in addressing these challenges. This study com-pares traditional GDI full-adder circuits with a proposed GDI-based full-adder circuit to achieve minimal energy consumption without com- promising performance. To validate the design, post-layout simulations are conducted on various GDI full adder designs using Cadence Virtuoso at the 45nm technology node. The results are then compared for area, power, and delay. Process corner and Monte Carlo simulations are also carried out on proposed and conventional GDI full-adder designs. Ultimately, the simulation results shows the energy value of the proposed 10T GDI Full Adder has decreased to 37.04% when com- pared to the current 10T GDI Full Adder. Then the proposed circuit is well-suited for low-power and high performance applications, making it a promising candidate for integration into energy-efficient systems.

**Keywords:** Full Adder, Power, Area, Delay, GDI.

Paper ID: 37

## Advanced Fault Detection in Cascaded H-Bridge Multilevel Inverters with LS-PWM Control

Ritika Roy, Sanskar Kumar Singh, Rupesh Shukla, Mr. Chandan Kumar Dr. A. Ambikapathy
Department of Electrical and Electronics Engineering, Galgotias College of Engineering and Technology

**Abstract:** The initial among these has become well-known due to its remarkable performance, and as a result, it is often used in greater voltage and higher electrical projects. Switch loss is more likely with this kind of inverter since changing semiconductor are utilized more often for power conversion. It is vital to find and identify these defects as soon as feasible as a result. A unique technique for detecting an open-circuit issue in cascaded H-bridge multilevel inverters (CHBMLIs) is described, using its level-shifted pulse width modulation (LS-PWM) technology. Unlike fault diagnosis methods, our methodology is simple and based on good logic to find errors by analyzing little issue characteristics. Analyzing the load voltage and the voltage at the output of the H-bridge are the two main components of the diagnostic procedure.

**Keywords:** Fault detection, Cascaded H-bridge multilevel inverters, LS-PWM control, Open-circuit fault, Diagnosis logic, Load current, Output voltage, Diagnostic variables, Detection time, Switching frequency.

Paper ID: 38

## A Double Sided Dielectric and p-GaN Gated GaN HEMT for Power Electronics Applications

Tanvika Garg, Sumit Kale
Electronics and Communication Engineering Department, Delhi Technological University New Delhi, India

**Abstract:** This paper introduces a novel enhancement mode GaN HEMT aimed at addressing gate leakage current issues. The device incorporates both a p-GaN layer and double sided Hf $O_2$ layers beneath the metal gate. The p-GaN layer functions as a barrier, effectively reducing tunneling effects, while Hf $O_2$ exhibits fewer trap sites in comparison to SiN, thereby leading to a decrease in gate leakage current. Additionally, the dielectric layers further contribute to the reduction of gate leakage current by adding another barrier between the gate electrode and the AlGaN layer. Also, a comparative analysis indicates that the proposed device demonstrates superior features, including improved gate leakage current, maximum drain current, and on-current, in comparison to the conventional p-GaN HEMT. Moreover, optimization techniques have been employed to achieve optimal device performance, with a specific emphasis on reducing gate leakage current. In addition, performance parameters of the proposed device have been compared with those of reported devices.

**Keywords:** p-GaN, Gate leakage, Dielectric layer and Optimization

Paper ID: 39

## Timing Constraint Check with Functional Verification of I2C Protocol Using Verilog

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**Abstract:** Since the inception of the inter-integrated circuit (I2C), many efforts had been made to enhance balance. Stability of the I2C device decrease due to timing errors. To overcome this error, we design I2C slave model using Verilog. The paper involves the verification of an I2C protocol implementation using Verilog, with a specific focus on ensuring that timing constraints are met while verifying the functional correctness of the design. The main aim of the paper is to do design and its verification using Verilog.

**Keywords:** Simulation, Functional verification, Timing errors, 12C Protocol, Verilog.

Paper ID: 40

## Using image processing Safety Helmet detection using YOLOV Technology in Indian road

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**Abstract:** At any site, where safety is a crucial factor and helmet is used for safety. It is important whether all workers or any individual is wearing helmet or not, to overcome this problem helmet detection project is proposed and it will help user to know about workers safety. To make accurate detection from long distances, complex background and among many targets, there is YOLOV-8 (you look only once version 8) which is the most upgraded model in yolov family. And it is known for its accuracy and speed. It detects targeted objects in real-time and non-real-time video frames. Training utilizes leading deep learning frameworks, dividing data for model development. Inference enables precise helmet detection and localization, with visualization enhancing result clarity. The system offers potential for real-time deployment in industrial safety, enhancing workplace safety and injury prevention. This research shows helmet detection by using YOLOV-8. The project totally depends on the algorithm YOLOV-8. It is an object detection algorithm which identifies the object and informs user accordingly.

**Keywords:** safety helmet, helmet detection, yolov8.

Paper ID: 42

## Design of low Power Highly Stable 9T SRAM in 22nm Technology

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**Abstract:** This paper explores low-power differential 9T SRAM cell in a 22nm-technology node using Monte Carlo simulations. All the Design Metrics for various SRAM configuration (conventional 6T SRAM and extended configuration standard 8T and our proposed 9T) are calculated and compared. Our Proposed 9T SRAM cell offers 11.4×/ 1.1× lower read access time and 14.7×/1.1× lower write access time as compared to conventional 6T and standard 8T SRAM cell respectively. In terms of leakage power our proposed 9T SRAM cell offers 12.7×/1.1×lower hold power, 5.2×/1.1× lower read power and 4.8×/1.1×lower write power as compared to conventional 6T and standard 8T SRAM cell respectively. We analyse the trade-offs between power consumption, overall performance, and reliability. The effects provide valuable guidance for selecting SRAM elements in energy-green electronic devices, ensuring low power consumption and data integrity, which are critical in advanced electronics.

**Keywords:** Read access time, Write access time, Hold power, Write power, Read power, SRAM cell.

Paper ID: 43

# Design and Parametric Analysis of an EBG Structure based UWB-MIMO Antenna with Improved Isolation for Connected Vehicle Technology

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Sri Vasavi Engineering College
Jerzy R. Szymański
Casimir Pulaski University of Radom
Marta Żurek-Mortka
Lukasiewicz Research Network-Institute for Sustainable Technologies
Mithileysh Sathiyanarayanan
MIT Square

**Abstract:** This paper primarily focuses on the design and parametric investigation of an Ultra Wide Band (UWB) antenna with Defected Ground Structure (DGS) loading, featuring a three-port Multiple Input Multiple Output (MIMO) configuration. Additionally, elliptical slots are etched on the ground plane to enhance bandwidth and isolation. Circularly slotted Electromagnetic Band Gap (EBG) structures are utilized to achieve these improvements in a compact UWB-MIMO antenna design. The proposed antenna has dimensions of 26×50×0.8 mm. From simulation results, it is observed that it exhibits extensive bandwidth from 3.6 GHz to 10.06 GHz, falling within the Ultra Wide Band category, and demonstrates an isolation of more than -43 dB. It is evident that the proposed antenna maintains good isolation even with a low end-to-end gap between patches of 8 mm. Key parameters assessing the antenna performance, such as radiation pattern, peak gain, surface current distribution, Total Active Reflection Coefficient (TARC), Envelope Correlation Coefficient (ECC), and Diversity gain, were investigated. The proposed system was designed on an FR-4 substrate with a dielectric constant of 4.4. The Proposed Antenna underwent evolution in five stages and was simulated using HFSS Software tool. The measured Envelope Correlation Coefficient (ECC) of the MIMO antenna was smaller than 0.002, the Diversity Gain (DG) was more than 9.98 dB, and the Total Active Reflection Coefficient (TARC) was -10 dB. To assess the reliable performance of the antenna in the presence of metallic bodies, the radiation characteristics of the antenna were also investigated when mounted on a vehicle using a CAD model of the car. The results show that due to its good performance and compact size, the suggested antenna is well-suited for high-throughput compact UWB transceivers in Connected Vehicle Technology and V2V Communication applications.

**Keywords:** MIMO, EBG, DGS, S11 Parameter, ECC, TARC, DG, Ultra-Wide Band, V2V.

Paper ID: 44

## Reduced Switched Multilevel Inverter as a Shunt Active Power Filter to Improve Power Quality

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Bikram Das
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**Abstract:** Recently, power electronics application in power system is very important. The parameters like power quality, stability, system reliability etc. can be improved by using power electronics devices like FACTS devices, active power filters etc. These devices are also important for efficient energy processing system, industrial automation, and conversion of electrical powers while satisfying the cost, size, reliability and life expectancy. In power system, customer side or distribution side is very important due to non-linear loads which produce current harmonics and it is a very important issue which needs to be attended carefully. The active power filters have capability to power quality improve and reactive power compensation. In this paper shunt active power filter is used for reducing harmonic content which is created by non-linear load. The reduced switched multilevel inverter as a shunt active power filter is used for eliminating the harmonics problem and in the retrieval technique. The complete task has been performed using Matlab simulation tool for the validation of the proposed idea.

**Keywords:** Multilevel Inverter, Shunt Active Power Filter, Harmonics, Power Quality Improvements.

Paper ID: 45

## Recessed-Gate AlGaN/GaN Based HEMT with Higher FT/FMAX for Millimetre-Wave Applications

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**Abstract:** In this paper, we present a gate-recessed GaN on SiC HEMT LNA for millimetre-wave and early terahertz band applications. Unique material selection, impurity injection and layer topology helped us achieve a unity current gain frequency (FT) of 679.2 GHz and a maximum oscillation frequency (FMAX) of 721.9 GHz with a current gain of 85 dB at 0.1 GHz. The proposed device exhibits an ultra-low minimum noise figure (NFMIN) of 0.053 dB at 10 GHz and 1.28 dB at the stern stability point of 179.7 GHz with off state gate leakage current in the picoampere range. The recessed-gate structure in the proposed model provides enhanced gate control of the channel carriers while reducing flicker noise characteristics by diminishing channel resistance fluctuation. The gate-recessing technique utilized in this work helps us supersede all latest GaN HEMTs vis-à- vis noise performance with our miniscule NFMIN and μS- range noise conductance in the millimetre wave frequency range. The effects of recessing and gate-channel distance on noise and amplification have been investigated superlatively in this work. The proposed GaN LNA can be integrated with MMIC layouts and with a Power Amplifier/ Radio Frequency (PA/RF) switch to form a compact GaN transmit/receive MMIC Solution.

**Keywords:** High electron mobility transistor (HEMT), millimetre-wave application, Monolithic Microwave Integrated Circuit (MMIC), transconductance (gm)

Paper ID: 46

## A Comprehension Review on HEMT for 6G Communication System

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**Abstract:** This comprehensive review explores the pivotal role of High Electron Mobility Transistors (HEMTs) in the context of 6G communication technology, aiming to provide an extensive overview for researchers and practitioners. HEMTs have garnered significant attention due to their unique electron transport properties, making them promising candidates for addressing the escalating demands of 6G networks. The review begins by elucidating the fundamental principles underlying HEMTs, emphasizing their high electron mobility and rapid operational capabilities. Subsequently, it delves into various design strategies and material considerations critical for optimizing HEMT performance in the specific context of 6G applications. This encompasses discussions on device architectures, semiconductor materials, and fabrication techniques, highlighting recent advancements. Furthermore, the review addresses key challenges associated with HEMT integration into 6G communication systems. Through a critical evaluation of existing solutions, the review proposes potential avenues for future research to overcome these challenges, enhancing the feasibility of HEMTs in 6G networks. The impact of HEMTs on crucial 6G communication parameters, such as data rate, spectral efficiency, and signal reliability, is thoroughly examined. Comparative analyses with alternative transistor technologies provide valuable insights into the distinct advantages that HEMTs bring to the evolving landscape of 6G communication.

**Keywords:** HEMT, 6G communication, GaN, Field plate, power amplifier, Transceiver system.

Paper ID: 50

## A Comparative Investigation into Voltage Mode, Current Mode and Charge Transfer Mode Sense Amplifiers

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**Abstract:** This research delves into a comprehensive comparison of three prevalent latched-based sense amplifier architectures concerning delay and power consumption per bit. The investigation includes a 6T SRAM cell with minimal size and a 128-bit SRAM column to enhance simulation realism. The outcomes reveal that the charge transfer sense amplifier exhibits superior performance in both delay and power consumption compared to its voltage mode and current mode counterparts. Supply and temperature sensitivity analyses further underscore the charge transfer sense amplifier's robust performance, particularly showcasing low delay variation with supply reduction, making it a favorable choice for subthreshold operation. Input sensitivity analysis indicates that the charge transfer sense amplifier outperforms in sensitivity, with lower offset compared to other architectures. These findings offer valuable insights for the design and implementation of sense amplifiers across diverse applications, emphasizing the potential advantages of the charge transfer sense amplifier in subthreshold and low-
power scenarios.

**Keywords:** SRAM, sense amplifier, scaled CMOS technology, voltage-mode sense amplifier, current-mode sense amplifier, charge transfer based sense amplifier.

Paper ID: 51

## A Low Noise Low Power Modified Folded-Cascode OTA for Neural Amplifier to detect Local Field Potential

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**Abstract:** Low Noise Amplifiers (LNAs) are important blocks of any biomedical application such as seen in caseof the analog front end (AFE) of a modern multichannel neural acquisition system where LNAs serve as the first stage immediately after the microelectrodes that sense bio signals produced by neurons. In this work a low power and low noise OTA based on the folded cascode topology is proposed as the core of a neural amplifier for the detection of local field potentials in the brain. Low noise is accomplished by utilizing source degenerated load which is implemented by employing three-stacked composite transistors. To meet power requirement, current scaling technique is exploited which aids in both circuit noise reduction and power efficiency. The OTA reports a high gain of 57dB and a very low flicker noise of 1.16μV/√Hz and an integrated noise of 2.9μV, power consumption of the proposed OTA equals 1.68μW while delivering a good CMRR of 83dB.

Paper ID: 52

## Optimization of Power and RF Performance using Oxide and Doping Engineering on Recessed Gate β-Ga2O3 MOSFET

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**Abstract:** In this study, comprehensive simulations have been conducted on β-Ga2O3 MOSFET with the aim of enhancing superior performance for high-power and RF applications. An exhaustive analysis of the proposed device encompassing analog characteristics, OFF-state and RF metrics has been carried out which is followed by its comparison with the conventional device to assess the efficacy of the proposed design. It is demonstrated that the proposed device not only outperforms conventional device in terms of analog and OFF- state metrics but also surpasses in RF performance. This research provides valuable insights and guidelines for utilizing the device across a wide spectrum of applications demanding high-power and RF capabilities.

**Keywords:** Gallium Oxide, High Power, High Frequency, Oxide Engineering, Doping Engineering.

Paper ID: 53

## Low profile, compact and simple design 2 port MIMO antennawith meander line as decoupling network for Vehicular communication

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**Abstract:** This article proposes a low profile compact two port MIMO antenna for safety band (ITS-5.9 GHz) which is commonly used in vehicular communication. It is very difficult to place a complex and relatively bigger size antenna in a vehicle for vehicular communication purpose to reduce the accident. To meet the requirement a 2 port MIMO antenna of size 40×20×1.58 mm3 with FR4 Epoxy substrate has been proposed. The antenna comprises of modified square patch with inset feeding technique. The meander line has been used as a decoupling network to reduce the mutual coupling between the closely spaced antennas which are 0.29λ apart from each other. The antenna shows an isolation value of 38.9 dB which is obtained due to the reduction of mutual coupling between the two elements radiators. The isolation has been improved due to the presence of a meander line. The peak gain recorded is 5.25dB at resonance frequency of 5.9 GHz.

**Keywords**: Vehicular communication; Mutual coupling reduction; Meander line.

Paper ID: 54

## Comparative study of Apoptosis process in Vertebrates and Invertebrates using Cytomorphic Approach

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**Abstract:** Apoptosis is a natural cell-suicide process, aiming at ensuring healthy life flow in both vertebrates and invertebrates. p53 protein, being 'guardian of genome', acts as the tumor suppressor in both classes of living organisms. In the present work, process of apoptosis in Drosophila is studied comprehensibly to formulate mathematical model and designing cytomorphic system of the process. For predicting the intra-cellular protein-protein interactions under stress condition, Ordinary Differential Equations (ODE) are formulated using Law of mass action. System model is designed for the entire biological process using Michaelis-Menten kinetics for studying the characteristics of the pathway in a quantitative manner. Each block of system model is converted into electronic system model using MOS-based low-power, low noise differential amplifier. The ODEs and system model are designed and simulated using MATLAB R2014a tool and circuit model is simulated using Cadence 0.18μm tool. Simulated responses of each participating protein resembles their biological nature. The simulation results are verified with previous biological experiments and observations.

**Keywords:** Apoptosis, Drosophila, Cytomorphic system, Differential amplifier.

Paper ID: 55

## Analysis of the Intricacies of Interfacial Trap Charge Distribution on Vertically Stacked Ferroelectric based FinFET for Improved Device Reliability

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**Abstract:** This paper examines the impact of localized charges on the Vertically Stacked Ferroelectric based FinFET, VS-FeFinFET's performance. The goal of this work is to comprehend how the interface trap charges created by radiation or stress-induced damage affect the performance of VS-FeFinFET in terms of various device parameters such as drain current, threshold voltage, transconductance, quality factor etc. These localized charges could have an impact on the transistor's operating point and circuit reliability thus the device has been studied with varying interface trap charge density in the range of $1 \times 1011 - 1 \times 1013$ with different polarity. With enhancement in some parameters like switching ratio by two times, output transconductance by 44.91% for negative polarity and degradation of some device characteristics in presence of positive interface trap charges, the analysis done in this study provides insights into the development of VS- FeFinFET with enhanced functionality, reliability, and performance, poised to shape the landscape of modern electronics.

**Keywords:** FinFET, Strained Silicon, Ferroelectric, Interfacial trap charge, Silicon on Insulator (SOI), Reliability.

Paper ID: 56

## Enhancing Energy Efficiency in Approximate Subtraction and Restoring Division for Error-Tolerant Systems

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**Abstract:** Approximate computing is a valuable method for applications that can tolerate errors, striking a balance between speed, power, and computational accuracy. This paper presents a novel approximate subtractor and its integration into diverse computing methodologies, including approximate restoring dividers employing triangle and horizontal replacement techniques, as well as ripple borrow subtractors. In this paper, the main objective is to compare the performance of the proposed subtractor with conventional approximate subtractors, focusing on power, area, delay, and power–delay product. Proposed approximate designs are implemented in Verilog HDL and simulated using the GPDK 90nm process in Cadence Software. To validate the proposed approximate subtractor, it is incorporated into an image blending algorithm using MATLAB software. The results are validated through error metric evaluation, specifically the peak signal-to-noise ratio (PSNR), when comparing conventional and proposed approximate subtractors.

**Keywords:** Approximate computing, Approximate dividers, Power, Area, Delay, Image processing.

Paper ID: 57

## ASIC-based Signal Conditioning Circuit Design for Biomedical Applications

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**Abstract:** Biomedical signals have very low energy and frequency range. In order to analyze these electrical signals and hence understand the physiological condition of a person's health, a low-voltage and low-frequency signal conditioning circuit is required. For remotely or regularly monitoring the health of a person, portable or wearable monitors that operate on ultra-low power is essential. The proposed work presents a low-power signal conditioning circuit that can cater to these portable or remote health monitors. The proposed circuit consumes 743.95 nW power, operating with a 1 V power supply and an input referred noise voltage of 3.00 μV/√Hz. The circuit has been simulated in the 180 nm technology of Cadance Virtuoso software and uses a two-stage CMOS-based Operational Amplifier with 14.62 dB gain and 8.93 pW power consumption with a 1 V supply. The overall circuit has been designed and validated for determining the heart rate from a person's photoplethysmography signal.

**Keywords:** Biomedical Signal Conditioning, 180 nm CMOS technology, Heart rate detection, Low power circuit, Low voltage application, Sub-threshold operation, Two-stage OpAmp.

Paper ID: 59

## Numerical Study on Impact of Sensing Film on modified ISFET for improved analog performance

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Abstract: This paper presents the comparative study of sensing layer of modified-ISFET with sensing film (Al2O3, Si3N4, SiO2) for analog and electrical performance. The dependent parameters are evaluated with variation in sensing material such as switching ratio that is enhanced by 3.5 times and leakage current which degrades by 63% at Al2O3 of modified ISFET, thus making the device suitable for high speed switching applications. Further it is found that the transconductance, device efficiency and sensitivity are also improved as compared to Si3N4, and SiO2 material. The improved electric field for Al2O3 makes the device more tolerant to high-temperature environments. The analysis displays better immunity of the device with Al2O3 in terms of power amplification and compatibility thus making the modified ISFET a potential candidate over conventional ISFET in field of bioelectronics.

Keywords— TCAD, ISFET, SS, Sensitivity.

Paper ID: 60

## Symmetric high-k spacer on S/D underlap Junctionless nanotube FET considering for cutting edge technology

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**Abstract:** The usage of III-V group semiconductors has increased drastically from the last few years owing to its superior characteristics that can be tailored by adjusting the composition and structure of the materials. In this paper, junctionless GAA nanotube FET has been studied with high-k spacer on S/D underlap region. The paper examines the device performance by incorporating the group III-V semiconductors such as GaAs, GaN and alloys such as InGaAs and SiGe. For this, comprehensive analysis has been done mainly in terms transfer characteristics, switching ratio, device efficiency, transconductance and its higher order, cut-off, and maximum frequency. The results obtained are simultaneously compared with silicon and found each of channel material has its own advantage. GaN exhibits superior performance in terms of high current driving capability, improved transconductance and its higher derivative, suitable for linear amplifiers. Further, InGaAs possesses low threshold voltage making it suitable for low power applications. GaAs achieves very low SS thereby possess high switching ratio. Thus, there is need to choose channel material wisely depending upon the applications.

**Keywords:** FET, Junctionless, underlap, linearity analog, HF.

Paper ID: 61

## r-GO/MoS2 Heterostructures Ultrasensitive Self-Powered Photodetector Operating in Both Narrowband and Broadband Regimes

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**Abstract:** We report tuning of spectral response from broadband (400 nm to 1100 nm) under high intensity illumination (Original light intensity) into narrowband (690 nm to 790 nm) under low intensity illumination (95% reduced intensity) of our ultrasensitive photodetector, at zerobias, with set of optical filters. In this work, the van-der Waals hetrostructure (r-GO/MoS2/p+-Si) is fabricated by using silver contact to the two r-GO parallel pads (reduced graphene oxide) drop casted on the multilayers of MoS2 grown on p+-Si substrate. The Multilayer 2H-MoS2 and r-GO pads growth are determined by Raman and XPS spectroscopy. The I-V characteristic of the device shows quasi-linear behavior in dark, ambient and light condition. Further, it exhibits high responsivity under light illumination of 690 nm wavelength with lowest power density (0.49 nW/cm2) are to be measured about 3.4 and 76.8 A/W, at 0V, and 0.2 mV bias respectively. The device shows fast photo response with measured rise time ~ 419 μs & fall time ~ 375 μs at 288 Hz chopper frequency. The fabricated device could be used for machine vision, imaging and short distance optical communication applications.

**Keywords:** Broadband response, Narrowband response, Heterostructures, MoS2, Reduced graphene-oxide,

Paper ID: 62

## Enhanced Session Key Generation and IIoT Device Authentication Mechanism for Secure Industrial Environments

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**Abstract:** With the advent of the Internet of Things (IoT), a ground-breaking communication technology, it is now possible to link devices with essential resources to the Internet. To remotely monitor and operate industrial applications, these devices are incorporated into a variety of industrial control systems. However, a major obstacle to the secure functioning of these systems is the public Internet's inherent susceptibility to hostile attacks. A lightweight and effective authentication mechanism is put forward as a solution to this problem. Using lightweight encryption operations, our proposed mechanism offers a comprehensive security solution that includes data integrity, secrecy, and authentication. Through message exchanges between the server, and smart embedded devices, it creates a secure channel that is necessary for the formation of a session key for safe data transmission. Thorough security analysis validates our proposed mechanism resilience, and performance analysis shows that it has a far lower operational cost and less communication overhead than other protocols. Our proposed protocol maintains robust security mechanisms that guarantee the confidentiality and integrity of data shared in the context of IIoT, even in spite of these efficiencies.

**Keywords:** Authentication, IIoT, Smart Device, Resource Constrained, Session Key.

Paper ID: 63

## Profiling of Dual Unit Induction Heating System with Multi Load by Asymmetrical Duty Cycle Control

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**Abstract:** Now a day's multiple load topologies for induction heating become advantageous over single load topologies due to uniform heat distribution. This paper presents a multi-load two-unit half-bridge inverter, where each unit consists of three loads. The asymmetrical duty cycle (ADC) control approach is used to operate each unit at the same switching frequency. The rate of heat flow has been modelled as a function of the current through the working coil, and the power of each unit can be individually adjusted. Thus, one can heat the required volume of the cylindrical solid workpiece. Multiple unit half-bridge topologies increase reliability and reduce the switching component count. Thus, the configuration is cost-effective. The proposed inverter configuration can be expanded to multiple loads and multiple units.

**Keywords:** Multiple loads, multiple units, half-bridge series resonant inverter, induction heating, asymmetrical duty cycle control, electromagnetic thermal equation, heat conduction.

Paper ID: 64

## Designing, Optimization and Statistical Analysis of Stack Oxide Junctionless FinFET based Ammonia Gas Sensor

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**Abstract:** This work presents, design and analysis of stack oxide junctionless FinFET (SO-JL FinFET) based ammonia (NH3) gas sensor. To detect the presence of NH3, Cobalt (Co) is used as catalytic gate electrode with stacking of SiO2/HfO2. The proposed device has been designed using Sentaurus TCAD simulator and to validate the simulation methods and models, the junctionless FinFET has been calibrated with the experimental results. The sensing performance of SO-JL FinFET NH3 sensor is demonstrated through change in work function of gate upon exposure to ammonia which eventually alters various sensing metrices of the sensor. Variation in surface potential and other electrical parameters such as threshold voltage (VTH), transfer characteristics, switching ratio (ION/IOFF), OFF current and threshold voltage sensitivity (SIOFF and SVTH respectively) have been analyzed at different values of Co gate work function. Simulation results reveal that proposed sensor exhibits high SIOFF of 5.65x103 and SVTH of 0.51 at work function change of 250 meV. Further, to optimize the SO-JL FinFET NH3 sensor the impact of variation of Fin width and Fin height on SIOFF and SVTH have also been investigated. Additionally, in order to examine the repeatability and stability of proposed device, statistical analysis of stack oxide junctionless FinFET NH3 sensor has been carried out to evaluate coefficient of variation of sensitivity parameters.

**Keywords:** SO-JL FinFET (stack oxide junctionless FinFET), Co (Cobalt), ammonia (NH3) gas sensor, statistical analysis.

Paper ID: 65

## Performance Investigation of Boost Converter using Adoptive Neuro Fuzzy Inference System and PI Controller

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**Abstract:** Power Electronics converters required robust and ingenious control for operating sophisticated instruments. DC-DC boost converters having wide applications in the field of power electronic circuits and renewable energy. In this paper design and analysis of closed loop-controlled DC-DC boost converter is performed with the application of adaptive neuro-fuzzy inference system (ANFIS). The main agenda of this design is to stabilize the output voltage by reducing the peak overshoot and minimize settling time during transient operations of proposed system and strengthen the performance in compare with conventional PI controller. At last, the same parameterized boost converter is tested for ANFIS controller and conventional PI controller in MATLAB Simulink environment and simulated results on resistive load are compared and correlated well.

**Keywords:** Boost Converter, PI Controller, ANFIS controller, Peak-Overshoot, Closed Loop Control.

Paper ID: 66

## Extended Huckel Model-based DFT Performance Analysis of GS-GNR FET for Low Power Applications

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**Abstract:** This paper reports the impact of the varied number of carbon atoms along armchair graphene nanoribbon (ACGNR) width (n) in the channel material of the gate stack graphene nanoribbon field effect transistor (GS- GNRFET). The transport properties using the Extended Huckel (EH) model-based density functional theory (DFT) approach is studied. The rise in 'n' from 4 to 7 enhances the on current (Ion), decreases off current (Ioff), improves the switching ratio (SR), and exhibits better transport properties like the device density of states (DDOS), transmission pathways (TP) and electron difference density (EDD). The improved findings of GS-GNRFET with n = 7 in channel material (A7) have significant potential for applications in low-power electronics, biomedical devices, and signal amplification areas.

**Keywords:** Density functional theory (DFT), Extended Huckel model, Low-power electronics, Transmission

Paper ID: 67

# PV Powered Contactless Charging Station for Electric Vehicles by Electromagnetic Induction

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**Abstract:** As a result of the encouragement received on electrical vehicles (EVs) by the government of India, the industry is bound to observe expeditious growth. This will significantly foster the increased manufacturing of electric vehicles, charging stations and also contactless power transfer devices for the sake of an efficient way to charge EVs. Owing to the fact that the EV market is experiencing rapid development, it becomes quite essential to overcome the shortcomings in the same. The establishment of an approach to charge the EV contactlessly will be appropriate since it has better convenience due to the exclusion of battery cost, recharge time and weight. This paper focuses on designing photovoltaic (PV) powered EV charging stations by electromagnetic induction. For high frequency contactless charging technique, a synchronous rectifier is also proposed in this paper. For higher output Voltage and frequency beyond 1 kHz, synchronous rectifier is extremely suitable. ANSYS Electromagnetics software has been used for the modelling of the practicability of the contactless power transfer approach for charging EVs by electromagnetic coupling. The charging of EVs through contactless power transfer (CPT) using the principle of electromagnetic induction is of apex concern on account of it being highly efficient and having higher power transmission capability and with immense charging distance. Additionally, the circuit diagram is illustrated with simulations of efficient transfer of energy between two coils which are magnetically coupled, using the PSIM software and Electromagnetics software.

**Keywords:** Contactless charging; PV Powered; Electromagnetic Induction, High Frequency, Synchronous Rectifier, Ansys Maxwell

Paper ID: 68

# Fraud Detection in Bank Payments Using SMOTE and Machine Learning Algorithms

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**Abstract:** This research introduces an advanced machine learning (ML) frame- work tailored for preemptive measures against bank fraud, specifically in the do- main of online transactions. Acknowledging the challenges arising from class imbalance in fraud datasets, our approach incorporates the Synthetic Minority Oversampling Technique (SMOTE) in the initial phase to enhance the model's adaptability and discrimination capabilities in the dynamic landscape of online fraud. In Stage Two, our methodology employs a heterogeneous ensemble comprising K-Nearest Neighbors (KNN), Random Forest, and XGBoost. KNN functions as an anomaly detector, identifying irregularities in transactional data. Simultaneously, Random Forest assesses feature significance and detects intricate patterns, contributing to a comprehensive understanding of fraudulent activity. XGBoost, known for its computational efficiency, ensures real-time responsiveness by adapting to emerging fraud tactics. Stage Three introduces a soft voting mechanism that seamlessly integrates individual algorithm predictions, resulting in a robust and highly accurate ensemble fraud detection system. Validation on an authentic bank fraud dataset underscores the framework's prowess, showcasing superior fraud detection capabilities and a significant reduction in false positives. This groundbreaking research enhances financial security and serves as a steadfast shield, safeguarding consumer assets amidst the evolving landscape of online fraud. In an era of digital evolution, our adaptable ML framework emerges as a potent tool for financial institutions, fortifying their defenses against criminal activities in the online banking domain.

**Keywords:** Machine Learning, SMOTE, Fraud detection, K-Nearest Neigh-bors, Random Forest, XGBoost, Classifiers

Paper ID: 70

## III-V Tunnel FET Biosensor: A Versatile Platform for Detecting Biological and Chemical Species

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**Abstract:** This paper reports a novel approach to detect biological and chemical species using a single nanocavity-etched Tunnel FET, leveraging its current voltage characteristics. By immobilizing biochemical species within the nanocavity, variations in dielectric constant induce significant changes in device properties, including threshold voltage, on current, and subthreshold swing (SS). The SILVACOATLAS device simulator is employed to obtain transfer characteristics of TFETs based on In0.53Ga0.47As, a low band gap and high mobility material. Voltage and current sensitivity are calculated using these characteristics. Optimization of the device structure, involving precise adjustments in doping concentration and source region thickness, yields remarkable voltage and current sensitivities of 3.32V and 1.935×108, respectively, showing improvement over the corresponding values reported earlier.

Paper ID: 72

## Bio-electricity generation by using green synthesized silver nanoparticles catalyst-based plant extract electrolyte solution

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**Abstract:** In this study, we developed four bio-electrochemical cells (BECs), each utilizing different electrolyte solutions. To enhance the electrical performance of these cells over time, we employed Colocasia esculenta extract, silver nanoparticles (Ag NPs), and a secondary salt to create distinct bio-electrolyte solutions. Employing a rapid, cost- effective, and environmentally friendly green synthesis method, we successfully generated Ag NPs by using Colocasia esculenta extract. The characterization of Ag NPs formation was conducted through XRD, UV-visible spectroscopy, FESEM, and FTIR. Applying the Ag NPs into the electrolyte solution, we observed comparative electrical performances across the four cells. The results indicated a significant decrease in internal resistance, accompanied by a noteworthy increase in average power and cell capacity. This study marks a groundbreaking advancement in improving the electrical efficiency of BECs by using Ag NPs.

**Keywords:** Biosynthesis, reducing agent, Ag NPs, BEC, electricity, power generation

Paper ID: 74

## A comprehensive study on the methods of optimization used in hybrid renewable energy systems

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**Abstract:** Use of all available energy sources is essential to meet the expanding demand for energy. The intermittent nature of renewable energy sources is a disadvantage even if they are clean, plentiful, and non-polluting. To address this problem, a hybrid energy system that combines renewable energies is used. This study presents and analyses in-depth literature evaluations of recently published studies on the topic of hybrid renewable energy. The study here does a review of hybrid system optimisation for renewable energy and presents its findings. This study carries out and then gives an assessment of HRES optimisation. The study also outlines the benefits and drawbacks of each optimisation technique.

**Keywords:** Hybrid renewable energy system, Optimization,Classical method, Artificial method, Hybrid method.

Paper ID: 76

## Effect of as composition fraction on sensitivity in dielectric modulated trench junctionless InAsxSb1-x DG FET biosensors

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**Abstract:** In this paper, we investigate the impact of As content on the performance of dielectric modulated InAsxSb1-x trench gate junctionless field effect transistor based biosensor using a well-calibrated simulation framework. The impacts are studied on the different performance indicators of the biosensor for detecting biomolecules having dielectric constants ranging 2.1-4.7. The results suggest that composition fraction of As has a strong influence on the sensing capability of biomolecules. Additionally, the findings reveal that the low composition fraction of As has more pronounced effect on biomolecules having higher
values of dielectric constants. The best result is obtained for a composition of 25% of As which is better than the Si channel devices.

**Keywords:** Biosensor, dielectric modulated JL FET, InAsSb channel, TCAD, sensitivity.

Paper ID: 78

## An Analysis On Wireless Power Transmission From Geo-Stationary Orbit To Earth Using PV Based Satellite System for Future Generation

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**Abstract:** Human beings can not think of a single step without electric power. From the past few decades with increase in population the demand of electrical power have also gone high and it will continue increasing in coming years. At present day most of these energies are obtained from non-
renewable sources such as, coal. If this continues the fuel reserves all around the world will get exhausted within the middle of this century, and as the demand of power is too high the renewable energy sources like solar energy, hydro energy, biogas energy, wind energy e.t.c., wouldn't be able
to meet the power requirements. Therefore, to circumvent with this problem, the following paper have been developed on an idea of wireless power transmission from the Geo-Stationary Earth Orbit using a space based solar powered satellite. For this objective, a satellite with a deployable large solar panel are used for generating power and transmit it to the ground station on earth through a microwave transmitter. While a rectifying antenna circuit on the ground station converts the microwave signal back DC.

**Keywords:** Wireless Power Transmission, Microwave, Geo-Stationary Orbit, Magnetron, Rectifying Antenna.

Paper ID: 79

## Digital Twin Technology: Exploring Frameworks, Challenges, and Resolutions

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**Abstract:** Digital twin technology generates a digital replica of a physical object or system and uses algorithms to integrate it within a virtual world. This enables real time simulation. With the ever-increasing amount of data due to industry 4.0, digital twin technology has emerged as a major player in reforming various industries. This is because of its ability to simulate, monitor and predict outcomes based on real world data with a high degree of accuracy. A lot of data is required to ensure the reliability and precision of the digital twin. This review paper discusses the standard framework and implementation steps used by this technology. Along with drawing attention to several concerns that are faced by this emergent technology. Furthermore, this paper discusses resolutions proposed by other papers to address these problems.

**Keywords:** Digital Twin, Standard Framework, Implementation Steps, Challenges, Security Concerns, Resolutions

Paper ID: 80

## Performance Analysis of FG-TFET for Future Ultra Low Power Applications

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**Abstract:** The main objective of this work is to enhance the performance of TFETs for ultra-low-power applications. Floating Gate Tunnel Field Effect Transistor is proposed to improving the ON current (ION), minimizing the OFF current (IOFF), reducing sub threshold swing (SS), and increasing the ION/IOFF ratio, Tranconductance (gm), and threshold voltage (Vt) are $12.2x10^{-11}$A , $1.14x10^{-17}$A , $3x10^{-8}$mV/dec, $10^{6}$, 3.33 $x10^{-11}$S, 0.4V. The work utilizes Gaussian doping to efficiently control the doping concentrations in TFETs. Gaussian doping is a technique used in semiconductor fabrication to create a controlled doping profile. The study involves using different materials, specificallysilicon (Si), germanium (Ge), andsilicon/germanium (Si/Ge) , for the gate of the TFET. The choice of gate material can have a significant impact on device performance. All simulation results in this work have been performed and obtained using Silvaco TCAD Simulation tool.

**Keywords:** TFET, ON current (ION), OFF current (IOFF), Subthresholdswing (SS), Ultra-low-powerapplications, Gaussian doping, 2D data.

Paper ID: 84

## 32-bit Carry Select Adder Design for High-Speed and Low-Power FPGA Applications

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**Abstract:** An optimized 32-bit Carry Select Adder (CSLA) design methodology for high-speed and low-power applications is presented. The design focuses on reducing critical paths and exploring non-uniform group sizes to improve performance. It also explores alternative multiplexing techniques for potential power/speed trade-offs. The methodology uses Verilog Hardware Description Language (HDL) and targets implementation on Intel Quartus Prime Lite software. The proposed design incorporates optimizations to achieve faster execution speeds compared to traditional CSLA, exploring technique like Carry Lookahead (CLA) and Carry Select mechanism for efficient carry propagation. The paper discusses design implementation, functional verification, and potential areas for further optimization based on the targeted Cyclone 10LP FPGA for Hardware validation.

**Keywords:** Carry Select Adder, Carry Lookahead, High- Performance Design, Verilog HDL, Quartus Prime Lite, Cyclone 10 LP FPGA.

Paper ID: 85

# Design and Implementation of an Automatic Test Equipment for testing Electromechanical Relay Parameters

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Department of Electrical & Electronics
Engineering Department of Mechanical
Engineering
National Institute of Technology Silchar,
INDIA Wabtec Corporation, Bengaluru,
INDIA

**Abstract:** Relays need to be fast to respond quickly to changes in input signals, ensuring timely switching operations. Faster operating times of relay helps in enhancing the overall efficiency and reliability of the system. To test such parameters some testing equipment's are needed. Therefore, oscilloscope is being used to test the switching time of the relays. But this approach is time consuming, and the price of the oscilloscope is very high. There is a need of minimal cost and time saving equipment to check the relay parameters. Therefore, an automatic test station is being prepared for measuring the electromechanical relay parameters using microcontroller with the help of an Arduino Mega 2560 Rev3 board. The main components of the proposed system are Arduino Mega 2560 Rev3 Board interfaced to a PC using USB cable and an electromechanical relay. The proposed test station is cost effective and time efficient. The parameters namely operating time, release time and bounce time are being measured by using this test station. This test station is cable of measuring parameters of both instantaneous and timer relay. The test station can measure the parameters of relay up to 6 contacts at once. The proposed test station reduces the cost up to 99.92% as compared to oscilloscope. The design of the system is based on combination of both software and hardware. The test developed was performed in Arduino IDE software. The result of the test is viewed in serial monitor of the Arduino IDE software. The hardware design is done in such a way that when the power supply is switched on the result will directly be displayed in the computer screen.

Keywords: Operating time, release time, bounce time, contacts, Arduino, microcontroller, cost effective, time efficient.

Paper ID: 88

# Design, Fabrication, and Characterization of System-on-Chips Accelerometer Using SOI Technologies: A Deep Dive into Secured Interfaces

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**Abstract:** Data protection received great attention due to security concerns. Owing to the increased demand for system security, System-on-Chip (SoC) accelerometer could serve many prospects with relevance to motion sensing and vibration sensing. This is because the principle behind the System- on-Chip (SoC) sensing can be measuring acceleration because they are suitable devices for vibrational analysis in complex systems. Designing such device that senses acceleration involves mainly the design of a proof mass that responds to such acceleration. Designing such proof mass proposes challenges with two aspects viz; design of a suitable geometrical structure and assigning relevant geometrical measurements that makes the proof mass suitable for operation in required predetermined specifications. The paper focuses on investigating and advising reasonable geometrical measurements and proposing a design, fabrication, and characterization of a silicon-on- insulator (SOI) SoC device, that is integrated in a metallic packaging and coupled to an optical fiber. In the integrated System-on-Chip (SoC) sensor, four specially engineered springs are integrated into the device layer, together with a mass structure and handle layers. For displacement interrogation, an optical reading system with a Fabry-Pérot interferometer (FPI) and a demodulation method is utilized. Because of its great sensitivity and immunity to electromagnetic interference (EMI), the (FPI) is also used. The results indicate that our designed SoC sensor exhibits a main resonant frequency of 1274 Hz with damping ratio of 0.0173 under running conditions up to 7 g, in agreement with the analytical model. However, our experimental findings show that our designed and fabricated SoC sensor when compared with other such designs has the potential for engineering application to monitor vibrations under high-electromagnetic environmental conditions

**Keywords:** Accelerometer; Cryptography; Fabry–Pérot interferometry (FPI); micro-electro-mechanical system (MEMS); silicon-on-insulator (SOI); System-on-chips (SoC); vibration Analysis

Paper ID: 92

## Comparative Analysis of Memristor-Inspired Digital Logic Circuits

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Nitin Sharma
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**Abstract:** Leon Chua predicted the memristor as another essential element for a circuit element in 1971. The first memristor was founded using TiO2. Memristors are essential for developing cutting-edge logic systems due to their compact size, low power consumption, and rapid processing speeds. They play a significant part in designing various digital circuits. Authors have anaysed memristor-based basic circuits like inverter, NAND/AND, NOR/OR, XNOR/XOR, and MUX. Circuits are designed using 180nm and 16nm CMOS technology transistors along with memesters. From the analysis of these circuits, it is concluded the effectiveness of memristors in optimizing the area, power, and speed of the gates as compared to traditional technologies.

**Keywords:** Memristors, CMOS, A14 Model, Gates, MUX, Delay, Power.

Paper ID: 94

## Design and analysis of low power CMOS SAR-ADC for Bio-Medical Applications

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**Abstract:** Accurate biological signal acquisition depends on very efficient SAR ADCs. In this work, biological signals are collected using an 8-bit CMOS 45 nm SAR-ADC. This work proposes a high energy efficiency in the nanowatt region by use of a DAC. Energy efficiency increases significantly since this technology makes comparisons possible without using any energy. According to the investigation, there is no requirement for particular offset cancellation methods; the comparator could potentially be optimized just by changing the transistor size. SAR-ADC design had been successfully realized employing 45 nm CMOS semiconductor technology. Spurious-Free Dynamic Range (SFDR) of 64.12 dB is achieved by the ADC at 1.89 microwatts of power consumption. Powering it is a 1 Volt voltage supply and it runs at a sampling rate of 1.1 Megahertz.

**Keywords:** SAR-ADC, DAC, CMOS

Paper ID: 95

## Alert System for Railway Worker Safety using Vibration Analysis and Mesh Networking with ESP32

Abhinav Agrawal, Adarsh, Abhinav Shukla
Supervisor : Prof. S. T. Nagrajan
Delhi Technological University

**Abstract:** Current railway safety measures for track maintenance often rely on manual lookout procedures, which are inherently unreliable and inadequate. This paper introduces a novel and comprehensive alert system designed to significantly improve worker safety. The system leverages strategically installed vibration sensors on rail tracks to detect approaching trains. The collected vibration data is processed by ESP32 microcontrollers. These ESP32 microcontrollers then analyze the signals for train presence. Upon detection, the ESP32 units trigger audible and visual alerts for workers.The ESP32 microcontrollers establish a self healing mesh network, enabling robust wireless data communication between nodes and ensuring reliable information dissemination across a wider coverage area. Additionally, the paper explores the potential of integrating machine learning algorithms for enhanced vibration pattern recognition. This advanced feature could enable the system to distinguish between different train types and potentially identify track faults through anomaly detection in long term vibration data. The system offers a significant advancement in railway worker safety by providing awareness of approaching trains, fostering a proactive approach to hazard prevention, and potentially contributing to improved track maintenance practices.

Paper ID: 97

## Prediction of Problematic Smartphone Usage Patterns Using WhatsApp Data

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Department, Punjabi University, Patiala, 147002, Punjab, India.

**Abstract:** Certainly, digital technological progress offers enormous benefits to the world, but these innovations have several dark sides. Due to the high facilitation offered by the smartphone, the society became highly dependent and addicted to smart- phone application usage. Excessive Smartphone Usage is a menace for modern society creating enormous social, psychological, health and lawlessness problems. There is an acute shortfall of studies on this issue. This study focuses on Prob- lematic Smartphone Usage behaviour patterns among users considering various demographic variables. To achieve the study aims, the WhatsApp status seen time data is collected from 189 participants for 128 days from Indian students representing different demographic backgrounds. To analyze the collected data, we employed descriptive statistics with various time series models, namely Auto-Regressive Integrated Moving Average (ARIMA), Prophet, and Long Short-term Memory (LSTM). The results posit that females are more prone to Problematic Smartphone Usage. The bachelor's degree students were found with a relatively higher risk of Problematic Smartphone Usage than their postgraduate and doctorate counterparts. Besides, the unmarried and unemployed are found with relatively higher Problematic Smartphone Usage than married and employed ones. Lastly, the results confirmed that the ARIMA forecasting algorithm is more efficient in forecasting behaviour than Prophet and LSTM. While Prophet algo- rithm gives better results than LSTM. The study findings can prove to be a better guide to the parents, psychologists, educators, social workers, and policymakers in understanding Problematic Smartphone Usage among students, who are the youth and future of the country.

**Keywords:** Problematic Smartphone Usage, Forecasting, Artificial Intelligence, Long Short-Term Memory Networks, Auto-Regressive Integrated Moving Average, Prophet

Paper ID: 98

## Implementing AES-256 key Algorithm on FPGA

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Vishwakarma Institute of Technology, Pune.

**Abstract:** The FPGA Implementation of 256 Bit Key AES Algorithm with Key Schedule and Sub Bytes Block Optimization project aims to enhance the efficiency and security of the Advanced Encryption Standard (AES) algorithm through FPGA technology. Leveraging insights from recent literature, the project explores optimizations in key schedule and sub bytes block operations. By integrating FPGA-based implementations, the project aims to improve AES encryption while optimizing hardware resources for secure data transmission.

**Keywords-:** FPGA, AES Algorithm, 256-bit Key, Key Schedule, Sub Bytes Block, Cryptography, Security, Data Encryption, Advanced Encryption Standard

Paper ID: 99

## Design of BLDC Motor Controller ASIC with Integrated Encoder Feedback

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**Abstract:** There are numerous applications for brushless DC motor driver systems, with an emphasis on improved control algorithms and system integration. Important problems that are necessary for dynamic applications like industrial automation and electric vehicle propulsion are being addressed by the research, including fault tolerance, torque ripple reduction, and sensor feedback operation. Utilizing MATLAB/Simulink and Arduino assistance to implement Model-Based Design concepts, the study suggests a low-cost method of streamlining development procedures. Various control strategies, such as PID control, closed-loop vector control, and Field-Oriented Control (FOC) using Space Vector Pulse Width Modulation methodology, is investigated. Additionally, novel PWM methods and FPGA-based controllers are being studied to improve system efficiency and control accuracy even more. In addition, the paper presents new discrete-component and ASIC-based sensorless controllers that handle commutation retardation and winding inductance issues. The efficacy and dependability of the suggested BLDC motor driver system are confirmed by simulation and experimental validation results, indicating that it is appropriate for a variety of commercial and residential uses.

**Keywords:** BLDC (Brushless DC Motor). Encoder, ASIC (Application Specific Integrated Circuit) Design, FPGA (Field Programmable Gate Arrays), PID (Proportional Integral Derivative)

Paper ID: 101

## Optimizing Breakdown Voltage and Performance of AlGaN/GaN HEMT via Recessed Height: Simulation Study

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Abhijit Bisws
Institute of Radio Physics and Electronics, University of Calcutta, Kolkata-700091, INDIA

**Abstract:** In this study, we introduce a high-electron-mobility transistor (HEMT) constructed with a super junction AlGaN/GaN design. Our aim is to optimize the device's breakdown voltage by varying the depth of the recessed region. Remarkably, we achieved a substantial breakdown voltage of 1.03 kV with a recessed height of just 5 nm. Furthermore, our findings show a significantly small value of ON resistance at this specific recessed height. Additionally, we meticulously assess various device parameters, including ON current, ON resistance, transconductance, and harmonic distortion, as part of our investigation.

**Keywords:** Super junction, breakdown voltage, current collapsing, harmonic distortion.

Paper Id: 102

## Design of Barrel Shifter using reversible logic

Abhay Chopde, Virendra Shelke, Kamlesh Shintre, Pratiksha Shinde
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**Abstract:** In this world of quantum computing, the advancements in reversible logic circuit designs are happening rapidly. This work introduces optimized designs for both 4-bit and 8-bit reversible unidirectional barrel shifters. The 8-bit version exclusively uses only 2:1 Reversible-MUX (RMUX) gate, but the 4-bit version combines the Feynman gate and 2:1 RMUX. The 4-bit barrel shifter achieves quantum cost (QC) of 28 and a garbage output (GO) count of 6, whereas the 8-bit version exhibits a QC of 96 and a GO count of 48. These innovative designs prioritize reduced quantum cost and unity fanout, demonstrating their efficiency in reversible logic applications.

**Keywords**: Reversible Barrel Shifter, RMUX, Reversible Logic, Quantum Computing, Quantum cost. pathways

Paper Id: 103

## FPGA Based Arrhythmia Detection Using Machine Learning

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**Abstract:** Arrhythmia poses a significant public health concern in India, where they contribute substantially to the high incidence of cardiovascular-related fatalities. Given that cardiovascular disorders account for approximately 28% of all deaths in the country, there is an urgent need for efficient and rapid arrhythmia detection technologies, especially in regions with limited access to modern medical infrastructure. This disparity is particularly pronounced between urban and rural areas, emphasizing the need for innovative solutions that can bridge this healthcare gap. Our project addresses this critical issue by integrating the parallel processing capabilities of Field Programmable Gate Arrays (FPGAs) with the predictive power of machine learning algorithms. Using Verilog-based programming, our system is designed to detect arrhythmias accurately and cost-effectively in real time with an accuracy of 90%. This approach not only enhances diagnostic capabilities but also makes advanced cardiac care accessible in underserved areas, thereby improving outcomes for a significant portion of India's population.

**Keywords**: Arrhythmia classification, FPGAs, Neural Network

Paper Id: 104

## Sensor based Surveillance System using Smartphone

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**Abstract:** This paper presents a novel approach to biometric gait identification using acceleration data from a mobile phone's built-in accelerometer placed in a trouser pocket. Unlike previous studies, we employ a Long Short- Term Memory (LSTM) network to analyze the acceleration data, which captures the complex patterns and rhythms in an individual's gait. Our experiment involves 21 volunteers aged between 18 and 20, and we achieve an accuracy of 85.7%. This approach leverages the unique patterns in an individual's gait to identify them, offering a promising solution for behavioral biometric authentication. The use of a mobile phone's accelerometer makes this approach convenient, non-intrusive, and widely applicable. The results demonstrate the potential of LSTM-based gait identification for various applications, including security, healthcare, and human-computer interaction.

**Keywords:** behavioural biometric; LSTM; gait identification; pattern recognition; mobile sensing; accelerometer.

Paper Id: 105

## Design and Implementation of ALU for16-bit single-cycle MIPS processor

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**Abstract**: The increasing need for faster and more powerful processors in different computing uses has created a demand for advanced architectures. Every processor has an essential element which is ALU within a CPU that ensures the processor's effectiveness. In response to the constant need for quicker computing architectures, this paper proposes the design and implementation of ALU for a 16-bit MIPS processor Using Verilog HDL and synthesizes it with the Xilinx ISE tool both of which leverage single machine cycle execution. The Arithmetic Logic Unit (ALU) is designed to support 29 R, I, and J-type instructions. With a 16-bit processor, this technology has its low power consumption, uncomplicated architecture, and great input/output control ability. Stimulation performance gives Clock period as 1000 nanoseconds with clock frequency of 1 MHz and execution time of 63 seconds.

**Keywords:** HDL, Verilog, ALU, MIPS Processor, 16-bit single cycle.

Paper Id: 488

## Sensing and Actuating Behavior of Jacketed PZT in Concrete subjected to 3.5 m Impact loading at 50º C Temperature

Indrajeet Singh, Shilpa Pal, Nirendra Dev
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**Abstract:** Structural Health Monitoring (SHM) is essential for the preservation and financial optimization of concrete buildings. The Electromechanical Impedance approach (EMI) has demonstrated potential as a method for Structural Health Monitoring (SHM) to monitor concrete damage. The study utilizes EMI approach to assess the structural integrity of concrete subjected to impact from a height of 3.5 m at a temperature of 50°C. During this experiment, concrete cubes were equipped with jacketed piezo sensors to capture their primary characteristics, namely conductance and susceptance. Prior to being subjected to loads, the concrete samples were heated to a temperature of 50°C. This was done to simulate the effects of temperature. After that, an iron ball was dropped from 3.5 m into the specimens. Also, PZT equivalent structural metrics like stiffness, mass, and damping were taken from the raw signatures to find changes in the specimens' mechanical properties. This helped us understand different damage conditions better. The experimental results show that jacketed PZT sensors are efficient actuating and sensing behaviour for concrete under impact and temperature loading.
**Keywords:** Electromechanical impedance technique; Piezo sensors; temperature loading; Impact Loading.

Paper Id: 112

## Pattern Recognition using Neural Network on FPGA

Abhay Chopade, Siddhant Tambatkar, Abaan Tamboli, Sanika Thorbole
VIT, Pune, Maharashtra, India

**Abstract:** This work presents a real-time pattern recognition system using neural networks which is implemented on Field Programmable Gate Arrays (FPGAs). The approach here uses a data acquisition and preprocessing pipeline to augment and extract video frame samples representing the four target symbols: blank circle, solid circle, plus, and cross. For this research a neural network architecture is thoroughly designed with a 7x7 input layer, optimally configured hidden layers, and four output nodes corresponding to each of the symbols. Rigorous training processes are used by using Octave scripts iteratively to optimize the network's weight matrix. The trained model is then converted into VHDL for seamless FPGA integration. The hardware implementation of this research leverages a stream processing strategy, introducing new pixels for each clock cycle for efficiently detection of the symbol.
Extensive simulations are carried out which demonstrate the accurate real-time pattern recognition having 91% accuracy. The FPGA's parallel computing capabilities have enabled high-speed processing of approximately 55 million pixels per second. This research has paved the way for robust, hardware-
accelerated pattern recognition systems with potential applications in various domains.

**Keywords:** FPGA, Neural Network, Pattern detection, Image processing

Paper Id: 113

# ANN Based Power Estimation for VLSI Circuits

Dr. Abhay Chopde, Mahek Zade, Shweta Wankhade, Sandesh Tangade
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**Abstract:** While designing integrated circuits, knowing the power dissipated in that circuit is important in order to optimize the design approach, leading to the optimal solution. The article proposes a novel method to estimate the power dissipated in a CMOS VLSI circuit, employing deep learning via an artificial neural network (ANN) as a regression model. The idea is to have a computationally less complex mechanism with greater accuracy. The proposed system achieves a high accuracy of 98.8% without needing high-end computational abilities. The model was trained and tested on a benchmark dataset, utilizing the MATLAB deep learning abilities. Moreover, the model has been quantized to reduce the computational complexity of the model. The system autonomously extracts essential circuit components responsible for power dissipation from the gate-level network. The proposed model was validated by implementing it on the FPGA Spartan 6 board, affirming its real-world applicability beyond simulations.

**Keywords:** VLSI, Deep learning, quantization, power estimation, netlist parser, FPGA, verilog.

## The Vidyasagar Awardee

The Vidyasagar Award is given to **Prof. Abhijit Biswas,** Professor, Department of Radio Physics & Electronics, University of Calcutta, Kolkata, West Bengal, India in 11th International Conference on Microelectronics Circuits and Systems. Micro2024 on 16th to 17th of May 2024. Organizer and Venue: Vinod Dham Centre of Excellence for Semiconductors and Microelectronics, Delhi Technological University, Rohini, Delhi-110042, India. Co-organizer: Applied Computer Technology, Kolkata, West Bengal, India.

## The Lotfi A Zadeh Memorial Awardee

The Vidyasagar Award is given to **Prof. Radhey Shyam Gupta,** Professor, Department of Electronics and Communication Engineering, Maharaja Agrasen Institute of Technology, Delhi, India in 11th International Conference on Microelectronics Circuits and Systems. Micro2024 on 16th to 17th of May 2024. Organizer and Venue: Vinod Dham Centre of Excellence for Semiconductors and Microelectronics, Delhi Technological University, Rohini, Delhi-110042, India. Co-organizer: Applied Computer Technology, Kolkata, West Bengal, India.

Micro2024, 16th – 17th May, 2024.
Organizer: Vinod Dham Centre of Excellence for Semiconductors and Microelectronics, Delhi Technological University, Bawana Road, Shahbad Daulatpur, Rohini, Delhi-110042, India.
Co-organizer: Applied Computer Technology, Kolkata, India
List of invited Speakers/ Session Chairs

| | |
|---|---|
|  | Keynote Speaker:<br>**Dr. Meena Mishra,**<br>Director, Solid State Physics Laboratory (SSPL), DRDO, Delhi, India. |
|  | Invited Speaker:<br>**Dr. Jacopo Iannacci,**<br>Centre for Materials and Microsystems (CMM), Fondazione Bruno Kessler (FBK), Trento, Italy. |
|  | Keynote Speaker:<br>**Prof. Jamal Deen,**<br>Distinguished University Professor, Director, Micro- and Nano-Systems Laboratory, Electrical and Computer Engineering Department, School of Biomedical Engineering, McMaster University, 1280 Main Street West Hamilton, ON L8S 4K1, CANADA, |
|  | Invited Speaker:<br>**Prof. Abhijit Biswas**<br>Professor, Department of Radio Physics & Electronics, University of Calcutta, Kolkata, West Bengal, India. And General Chair (Publication, Micro2024). |
|  | Keynote Speaker<br>**Prof. Abhinav Kranti,**<br>Professor, Department of Electrical Engineering, Indian Institute of Technology, Indore, Madhya Pradesh, India. |

| | |
|---|---|
|  | Invited Speaker<br><br>**Prof. Mridula C Gupta,**<br><br>Professor, Department of Electronic Science, University of Delhi, South Campus, South Moti Bagh, New Delhi, Delhi, India - 110007 |
|  | **Dr. Moumita Mukherjee**<br><br>Dean (R & D), Adamas University, Barasat, Kolkata, West Bengal,India.<br>(Ex. Sr. Scientist of DRDO Centre of Excellence) (under Ministry of Defence, Govt. of India). |
|  | Invited Speaker<br><br>**Prof. Mukul Sarkar,**<br><br>Professor, Department of Electrical Engineering, Indian Institute of Technology, Delhi, India. |
|  | Invited Speaker<br><br>**Dr Hab. Eng. Piotr Bojarczak,**<br><br>Professor, Faculty of Transport, Electrical Engineering and Computer Sciences, URad Casimir Pulaski University of Radom, POLAND. |
|  | Invited Speaker<br><br>**Dr. Ashwini K Aggarwal,**<br><br>Director, Applied Materials India Pvt. Ltd., Faridabad, Haryana, India. |
|  | Invited Speaker<br><br>**Dr. Mukesh Jewariya,**<br><br>Senior Scientist, National Physical laboratory, CSIR (Council of Scientific and Industrial Research), Delhi, India. |

| Organizers | Name/Affiliations |
|---|---|
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|  | Convener(s):<br>Dr. Mohan S. Mehata:<br>Department of Applied Physics, Member, Vinod Dham Centre of Excellence for Semiconductors and Microelectronics, Delhi Technological University, Delhi. |
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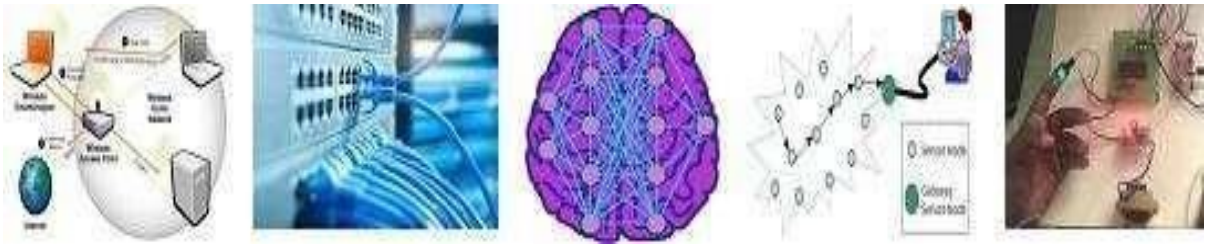

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