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A Comprehensive Review of Active two phase Charge Pump Topologies for Low Current Applications

Jayesh Joshi, Aastha Gupta, Rishabh Badjatya, Sneha Suhagir, Vaibhav Neema

Department of Electronics and Telecommunication Engineering
Institute of Engineering and Technology, DAVV, Indore, INDIA
Corresponding Author: jayeshh6565@gmail.com

ABSTRACT

This work provides a comprehensive evaluation and comparison of various active two-phase charge pump voltage multiplier topologies for low-current and high-voltage applications. Topologies studied include Dickson, series-parallel, cross-coupled, exponential, and Fibonacci charge pumps. All circuits are simulated with 180 nm CMOS technology to generate an output voltage of around 5 V from 1.8 V input. The performance is measured using essential metrics such as rise time, power dissipation, voltage conversion efficiency (VCE), power conversion efficiency (PCE), and area. The results indicate that the cross-coupled architecture achieves the best efficiency with VCE of 96.33% and PCE of 71% while consuming less power and having fewer stages. The series-parallel topology provides the quickest response, while the Fibonacci structure offers minimal area. A figure of merit (FoM) is introduced for the overall comparative analysis, showing that the cross-coupled architecture performs best. This study supports the selection of appropriate charge pump topologies for low-power integrated applications like IoT systems, biomedical devices, energy harvesting circuits etc.

Keywords: Charge Pump, Power Conversion Efficiency, Voltage Multiplier, Voltage Conversion Efficiency.

I. INTRODUCTION

The need for effective voltage boosting methods has grown significantly due to the rapid development of modern electronic systems, especially in low-power and portable applications. Non-volatile memory, RF modules, analog circuits are some of the functional blocks in many integrated circuits that cannot be driven by the available supply voltage [1]. To resolve this constraint, voltage multipliers, also known as charge pumps, are frequently used as efficient DC-DC converters capable of producing greater output voltages from low input voltages [2]. Charge pumps are voltage conversion circuits that use capacitors and switches rather than inductors, making them ideal for CMOS implementation. This allows small sized design, low cost, and easy integration within the system [3]. As a result, they are commonly used in a variety of applications, including energy harvesting systems [4], implantable biomedical devices [5], on-chip biasing circuits [6], Internet of Things (IoT) devices [7], and wireless sensor networks [8]. Most of such applications need circuits that are capable of producing high output voltage while working at low current levels with quick reaction which makes the charge pump design especially important.

The operation of a charge pump can be described using a functional block approach as shown in Fig 1. The input source, which may be an AC signal or a clock-driven DC input, provides the initial energy.

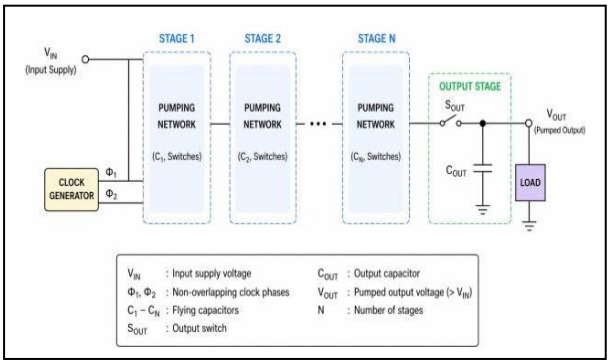

Fig. 1. Charge Pump Voltage Multiplier Architecture (1, 2 ...N stage)

In switched-capacitor implementations, a clock/control block generates non-overlapping phases to regulate switching. The charging network comprises capacitors and MOS switches which store energy during the charging phase and transfers it across successive stages. The capacitor voltages in each stage are essentially accumulated in series, resulting in a higher output from voltage multiplication. An output filter capacitor helps to smooth the fluctuating voltage leading to a stable DC output. Finally, the increased voltage is applied to the load [9]. Charge pump circuits have grown from simple diode-based architectures to complex MOS-based topologies as supply voltages raised with greater demand for energy-efficient solutions. These advanced MOS-based topologies increase voltage gain, lower power dissipation, and improve overall efficiency [6]. However, choosing the optimum architecture for a specific application remains difficult due to trade-offs between performance metrics. The paper is structured as follows: Section II discusses the classification of voltage multipliers. Section III presents the results and analysis

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of the Dickson, Series-Parallel, Cross-Coupled, Exponential, and Fibonacci Charge Pump Topologies. Section V includes overall conclusion of the presented work.

II. CLASSIFICATION OF VOLTAGE MULTIPLIERS

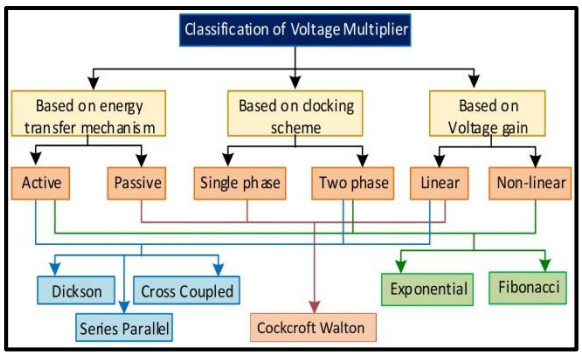

Fig. 2. Classification of Voltage Multiplier

As illustrated in Fig. 2, the voltage multipliers are widely categorized according to energy transfer techniques, clocking schemes, and voltage gain. The multiplier can be either active or passive depending on the energy transfer technique. The only components of passive voltage multipliers are diodes and capacitors. These multipliers usually function at lower frequencies. On the other hand, Active voltage multipliers use MOSFET switches with capacitors and clock signals to operate at medium to high frequencies with better performance. The multiplier can be either single phase or two phases driven depending on the clocking system. A two-phase voltage multiplier uses two non-overlapping clock signals for controlled and effective operation, while a single-phase voltage multiplier utilizes one clock signal for charge transfer [3]. A voltage gain multiplier may be either linear or non-linear. The output voltage of non-linear multipliers increases non-linearly and that of linear multipliers increases proportionally with the number of stages.

The Cockcroft Walton voltage multiplier [10] is categorized as a passive, single-phase multiplier since it uses diodes and capacitors without actively driven switches. Dickson [11], series-parallel [12], cross-coupled [13], Fibonacci [14], and Exponential [15] charge pumps are classified as active, two-phase voltage multipliers because they employ clock-controlled MOSFET switches. In terms of voltage gain, Cockcroft Walton, Dickson, series-parallel, and cross-coupled are linear multipliers, while Fibonacci and Exponential are nonlinear multipliers. This work provides stronger emphasis on active two-phase charge pumps since they perform better in terms of efficiency and reduced voltage loss for low-voltage CMOS implementation. These properties make them better suited for applications that require low power consumption, high voltage gain, and quick dynamic response.

A. Active, Two Phase Charge Pump Voltage Multiplier

1. Dickson charge pump: The Dickson [11] is linear charge pump which employs a cascade of capacitors and diode-connected MOSFETs driven by two alternating clock phases. In one phase, the capacitors charge from the input supply (Vin), and in the next, this stored charge is transferred to subsequent stages (N), progressively boosting the output voltage ($Vout$). Each stage contributes an incremental voltage increase, resulting in a higher overall output with more stages. However, the performance is limited by threshold voltage (Vth) drop across the MOSFETs. The output voltage for Dickson charge pump is given in Equation (1).

$$V_{out} = V_{in} + (V_{clk} - V_{th}) \quad (1)$$

2. Series-Parallel charge pump: The series–parallel [12] is linear charge pump which operates by alternately reconfiguring capacitors between parallel and series connections. During the charging phase, capacitors are connected in parallel to the input source and charged to the same voltage. In the subsequent phase, they are switched into a series configuration, causing their voltages to add and thereby boosting the output. The output voltage for Series-Parallel charge pump is given in Equation (2).

$$V_{out} = N\, V_{in} \quad (2)$$

3. Cross-Coupled charge pump: The cross-coupled [13] is linear charge pump which utilizes a pair of cross-connected MOSFETs, capacitors, and two non-overlapping clock signals to enable efficient charge transfer. During operation, complementary switching ensures that one set of MOSFETs conducts while the other turns off, resulting in alternate charge transfer between stages. These configurations effectively minimize threshold voltage loss and improve charge transfer efficiency. The output voltage for Cross-Coupled charge pump is given in Equation (3).

$$V_{out} = V_{in} + N\, V_{clk} \quad (3)$$

4. 2^N Charge Pump: A 2^N charge pump is [14] is non-linear architecture which operates by first charging capacitors to the input voltage and then reconfiguring them through MOSFET switches so that their voltages combine multiplicatively rather than add incrementally. During each clock cycle, capacitors are stacked with the input or previous stages, producing a large voltage increase. Repeated switching leads to a rapid, exponential rise in the output voltage. The output voltage for Exponential (2^n) Charge Pump is given in Equation (4).

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$$V_{out} = 2^N V_{in} \quad (4)$$

5. Fibonacci Charge Pump: The Fibonacci is non-linear charge pump [15] that uses capacitors whose values follow the Fibonacci sequence along with switches and clock signals. During operation, in one clock phase, the capacitors are charged from the input supply. In the next phase, the stored charge is transferred to the following stages. Since the capacitor values increase according to the Fibonacci pattern (F_n), more charge is transferred in the later stages. The output voltage for Fibonacci Charge Pump is given in Equation (5).

$$V_{out} = V_{in} + \sum F_n V_{in} \quad (5)$$

III. RESULTS and DISCUSSIONS

The design and simulation of various active two-phase charge pumps circuits were carried out using the Cadence Virtuoso platform with SCL 180 nm CMOS technology. A comparative analysis is performed to reach the output voltage ≈ 5V based on key parameters, including power dissipation, rise time, area and efficiency.

(i) Power dissipation: Power dissipation refers to the total power consumed by the circuit during operation. From the analysis, it is observed that the cross-coupled topology exhibits the lowest power dissipation of 31.16 µW among all the configurations due to elimination of threshold voltage losses, efficient charge transfer and reduced number of stages, while the remaining topologies show nearly comparable power consumption. The power dissipation of all multipliers configurations is tabulated in column V of Table 1.

(ii) Rise time: Rise time (tr) is defined as the time required for the output voltage to increase from 10% to 90% of its final steady-state value. The results indicate that the series–parallel topology exhibits the minimum rise time of only 14 µs due to simultaneous parallel charging, and faster charge transfer with reduced propagation delay, followed by the cross-coupled configuration, whereas the Fibonacci topology requires the longest time of 70 µs to reach its steady-state value due to its gradual and uneven charge transfer mechanism. The rise time of all multipliers configurations is tabulated in column VI of Table 1.

(iii) Voltage Conversion Efficiency: Voltage Conversion Efficiency (VCE) is defined as the ratio of the practical output voltage to the ideal or expected output voltage as given in Equation (6). It is observed that the cross-coupled charge pump achieves the highest VCE of 96.33%, followed by the exponential topology at 80.3%, whereas the Dickson charge pump exhibits the lowest VCE of 50.09%. The VCE of all multipliers configurations is tabulated in column VII of Table 1.

$$VCE = \frac{V_{out}}{V_{Ideal}} * 100\% \quad (6)$$

(iv) Power Conversion Efficiency: Power Conversion Efficiency (PCE) is defined as the ratio of output power to the input power as given in Equation (7). The PCE is mentioned in column VIII of Table 1. It can be observed that cross-coupled leads all other architectures with highest 71% PCE due to reduced threshold losses and efficient charge transfer whereas Dickson lags all others with minimum of 12% due to cumulative threshold voltage drops and inefficient charge transfer across stages.

$$PCE = \frac{P_{out}}{P_{in}} * 100\% \quad (7)$$

(v) Area: The area of the multiplier is evaluated based on the total length and width of all stages which includes MOS transistors and on-chip capacitors. The results indicate that the Dickson topology requires a larger number of stages to achieve the desired output voltage due to successive threshold voltage drops at each stage, leading to the highest area consumption of 1.02 mm². In contrast, the Fibonacci topology occupies the least area (approx. 0.08 mm²) due to the requirement of fewer stages and smaller-sized capacitors.

(vi) Figure of Merit: The Figure of Merit (FoM) is introduced to evaluate the overall performance of active two-phase charge pump architectures considered for comparison. Based on the important performance parameters it is defined as the ratio of the product of PCE and output voltage to the product of power dissipation area and rise time as given in Equation (8).

$$FOM = \frac{V_{out} * PCE}{t_r * PD * Area} * 1000 \quad (8)$$

The performance comparison of different active two-phase charge pumps circuits for 1 MΩ load at 1 MHz is presented in Table1.

Fig. 3 shows the variation of output voltage with four different load resistance (100KΩ, 500KΩ, 1MΩ and 2MΩ) for different charge pump architectures. The cross-coupled and series-parallel architectures exhibit superior load regulation, maintaining a nearly constant output over a wide range of load resistance. In contrast, the remaining architectures show significant output variation, indicating poor load stability.

Fig. 4 illustrates the variation of voltage conversion

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efficiency (VCE) with the number of stages. VCE is calculated by the equation 6.

TABLE I. PERFORMANCE METRICS OF CHARGE PUMP TOPOLOGIES INCLUDING VOUT, EFFICIENCY, POWER AND AREA

Topology	Input voltage Vin (V)	Output voltage Vout (V)	No. of Stages (N)	Power Dissipation (µW)	Rise Time Tr (µs)	Voltage Conversion Efficiency VCE (%)	Power Conversion Efficiency PCE (%)	Area (mm^2)
Dickson	1.8	5.184	6	51.98	45	50.09	12	1.02
Series-Parallel	1.8	5.074	3	52.51	14	74.61	38.3	0.25
Cross-Coupled	1.8	5.173	2	31.16	22	96.33	71	0.30
Exponential (2^n)	1.8	5.539	2	48.13	32.5	80.3	38.3	0.15
Fibonacci	1.8	5.102	3	51.38	70	70.11	34	0.08

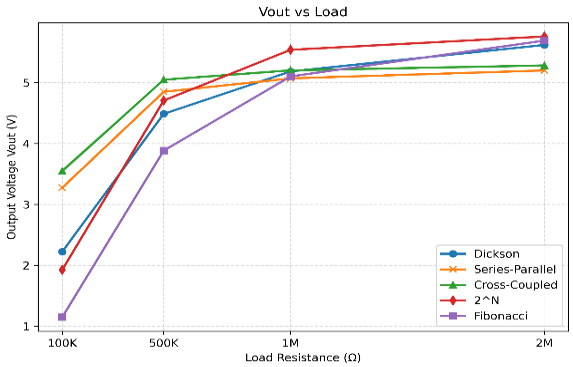

Fig. 3. Variation of output voltage w.r.t. Load resistance

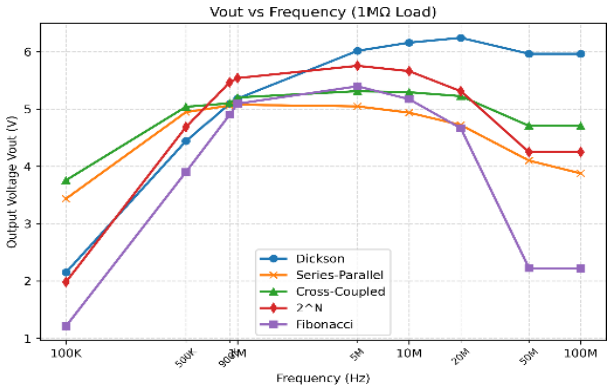

Fig. 5. Variation of output voltage w.r.t. frequency

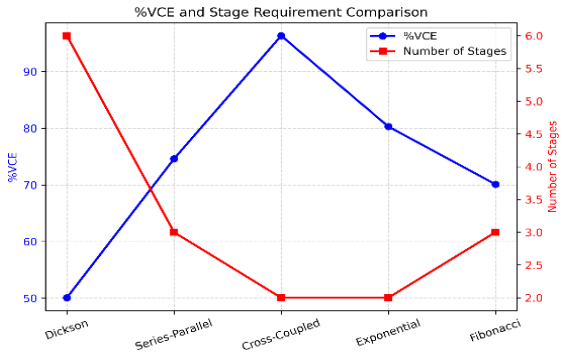

Fig. 4. Voltage conversion Efficiency and number of stages for various multiplier architectures

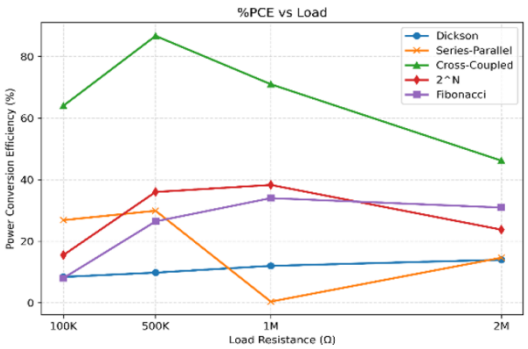

Fig. 6. Variation of Power Conversion Efficiency w.r.t. Load

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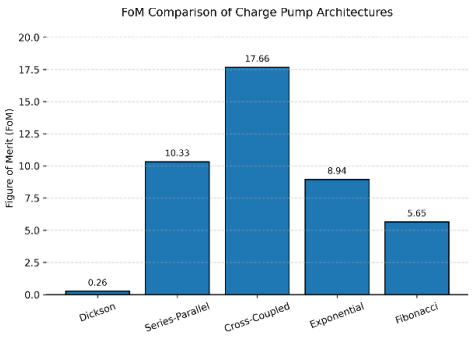

Fig. 7. FOM Comparison of various charge pump architecture

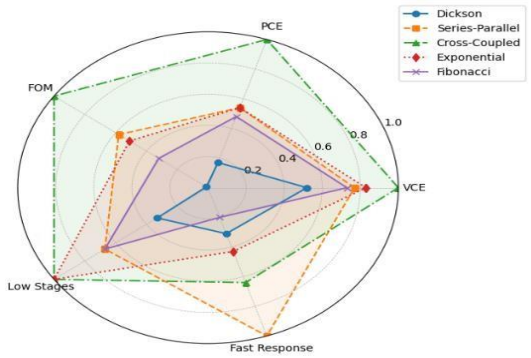

Fig. 8. Radar plot for different architectures based on VCE, PCE, FOM, number of stages, and response speed.

The cross-coupled architecture achieves the highest VCE with the minimum number of stages, highlighting its efficiency in voltage boosting. The 2^N architecture follows with comparatively lower VCE under similar conditions. In contrast, the Dickson architecture demonstrates poor VCE despite requiring a higher number of stages, reflecting its reduced efficiency.

Fig. 5 presents the variation of output voltage with frequency. The cross-coupled and series-parallel architectures maintain a stable output across a wide frequency range, whereas other architectures exhibit noticeable dependence on frequency, leading to output fluctuations.

Fig. 6 shows the variation of power conversion efficiency (PCE) with load resistance. The cross-coupled architecture provides maximum PCE with load resistance of 500 kΩ. The Dickson architecture has minimum PCE but is relatively insensitive to load variations. Conversely, the series-parallel architecture exhibits significant change in PCE with varying load, showing a greater sensitivity to load.

Based on the results obtained, the advantages and drawbacks of various charge pump architecture are analyzed which are tabulated in Table 2

TABLE II.
ADVANTAGES AND DRAWBACKS OF VARIOUS CHARGE PUMP ARCHITECTURES

Topology	Advantage	Disadvantage
Dickson	Simple, stable	Require large no. of stages, high power dissipation and least efficient.
Series-Parallel	small rise time, less no. of stages required	High power dissipation, low PCE
Cross- Coupled	Low power dissipation, rise time, less no. of stages required and very high VCE and PCE	Rise time is slightly higher
Exponential (2^n)	less no. of stages required, high VCE	High power dissipation, low PCE
Fibonacci	less no. of stages required, occupy small area	Very high rise time and power dissipation, low PCE

The Figure of Merit (FoM) for various architectures is presented in Fig. 7. It can be observed that the cross-coupled topology achieves the highest FoM due to its combination of low power dissipation, high output voltage, low rise time, and compact area. In contrast, the Dickson topology exhibits the lowest FoM, as it underperforms across all considered parameters, leading to degraded overall performance.

The radar plot as shown in Fig. 8 compares different voltage multiplier architectures based on VCE, PCE, FOM, number of stages, and response speed. The cross-coupled shows the best overall performance, with the highest efficiency (VCE and PCE), highest FOM, and fewer stages. The series-parallel also performs well and provides the fastest response, making it suitable for high-speed applications. The exponential and Fibonacci show moderate performance across all parameters. In contrast, the Dickson architecture has the lowest efficiency and overall performance. Overall, the cross-coupled architecture offers the most effective design among the compared topologies.

IV. CONCLUSION

This work presents a detailed comparison of different charge pump voltage multiplier architectures based on simulation results and performance metrics. Among all the considered topologies, the cross-coupled charge pump demonstrates the best overall performance, offering high efficiency, low power dissipation, fewer stages, and a high figure of merit. The series-parallel architecture is suitable for applications requiring fast response, while

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the Fibonacci topology is advantageous in terms of compact area. The exponential topology provides moderate performance, whereas the Dickson architecture shows the lowest efficiency and requires more stages, making it less suitable for modern low-power applications. However, for most low-current and high-voltage applications, the cross-coupled architecture emerges as the most effective solution.

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