

Low-Power Optimization of an FSM-Based Elevator Controller System

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ABSTRACT

Power consumption is a critical concern in contemporary Very Large-Scale Integration (VLSI) systems owing to increasing demand for energy-efficient electronic devices. Reducing power while maintaining system performance is an important objective in digital circuit design. This paper describes the design and low-power optimization of an elevator controller based on Finite State Machine (FSM) implemented in the Register Transfer Level (RTL). The controller manages elevator operations such as floor requests, movement, and emergency stop using a structured FSM architecture. The suggested design uses various low-power methods, such as power-aware state encoding with gray code and gray encoding with clock gating to lower the total amount of dynamic power used. The Xilinx Vivado suite is used to construct the suggested design in Verilog. According to empirical analysis, every method helps to lower dynamic power. In comparison to the baseline design, the improved design reduces total on-chip power by 36.69 % and dynamic power by 39.0 %. The findings show that the power efficiency of FSM-based elevator controller systems may be enhanced by combining several low-power strategies while maintaining functionality.

Keywords: State encoding, Elevator controller, Low-power VLSI architecture, Clock gating, Finite state machines.

I. INTRODUCTION

The need for low-power digital integrated circuits has grown substantially due to the swift development of semiconductor technology and portable electronics. Power consumption has become one of the most significant design challenges in modern Very Large-Scale Integration (VLSI) systems. Because of various factors like battery capacity, thermal limits, and the growing complexity of digital circuits. With scaling of device density following Moore's law, power dissipation becomes a serious issue in thermal dissipation, packaging, and battery life [1].

Therefore, establishing efficient design for energy savings purposes at Register Transfer Level (RTL) stage of the development process becomes a key area of study.

A wide variety of digital applications, such as embedded control units, industrial automation, and communication protocols, rely on finite state machines (FSM) as its basic control framework [2]. One of the classic examples of such a control unit would be the one that manages an automated FSM-based elevator, which must manage floor request, high-priority emergency, and real-time motor coordination [3]. Power consumption in digital design is predominantly caused by switching in combinational and sequential logic. Conventional FSM designs using binary state encoding often result in higher switching transitions, leading to increased dynamic power consumption [4]. To address this issue, Gray encoding can be utilized, where only one-bit changes between consecutive states, thereby reducing unnecessary transitions and lowering power dissipation [5]. In addition to encoding techniques, power optimization methods such as clock gating are widely used in low power techniques. clock enable signal are used to minimize switching activity. Clock gating prevents unnecessary updates in flip-flops [6].

This work presents the design and low-power optimization of an FSM-based elevator controller implemented at the RTL. The controller includes four operational states: IDLE, MOVING_UP, MOVING_DOWN, and EMERGENCY, which manage elevator movement based on floor requests.

The design is implemented and verified using simulation tools, followed by synthesis and power analysis. Several low-power techniques, including power-aware state encoding and state encoding with clock gating are applied to reduce dynamic power consumption [7].

The experimental results demonstrate that the combination of these techniques significantly reduces overall power dissipation while maintaining correct system functionality. The proposed optimized design achieves a substantial reduction in dynamic power compared to baseline design, highlighting the effectiveness of low-power design strategies in FSM-based digital systems.

The rest of this paper is structured as follows: Section II presents the literature review, section III provides the

design and methodology, section IV depicts design without low power optimization techniques, section V shows design with power-aware state encoding, section VI illustrates design with power-aware state encoding and clock gating, section VII shows results and conclusion is given in section VIII.

II. LITERATURE REVIEW

The growing demand for energy-efficient digital systems has led to extensive research in FSM optimization and low-power hardware design. This section provides an overview of existing methodologies in elevator control systems and various RTL-level power reduction techniques. FSM are widely used in control applications because they offer predictable behavior and are easy to design and implement. Anreddy [8] proposed elevator control system using FPGA, demonstrating efficient handling of multi-floor requests and improved response time. In a similar way, kumar [3] demonstrated that FSM-based systems are appropriate for creating efficient control system designs by designing an elevator controller using Verilog HDL. Such research works have proven the efficacy of FPGA platform for developing elevator controllers.

The switching activity of FSMs, which precisely affects dynamic power consumption, is generally determined by state encoding. Vaibbhav and Taraate [4] provided a state encoding methodologies and validated that higher switching activity results from multiple bit transitions between states caused by standard binary encoding. To solve this problem, Gray encoding is extensively used since it guarantees one-bit change between successive states. Y. P. Dwivedi and S. Kumar [5] explained that Gray encoding techniques effectively decrease power dissipation in FSM-based systems by eliminating redundant changes. This method is advantageous when implementing FSMs on FPGAs, where power dissipation is attributed mainly to switching behavior. Clock gating is considered one of the most effective RTL-level approach for reducing dynamic power consumption. Jasmin, M. [6] proposed a method that combines state encoding with clock gating to reduce switching activity in sequential elements. Bezati [7], Shinde [9] and Aruna [10] discussed modern trends in energy-efficient digital circuits, highlighting the importance of reducing switching activity and optimizing clock distribution. Additionally, Recent research emphasizes the integration of multiple power optimization techniques to achieve maximum efficiency.

However, most of the existing work focuses on individual techniques, and limited research addresses their combined application specifically for FSM-based elevator control systems on FPGA. Therefore, this work aims to integrate power-aware state encoding with clock

gating to achieve enhanced power efficiency in an FSM-based elevator controller.

III. DESIGN and METHODOLOGY

This work introduced the design and implementation of a low-power FSM based elevator controller utilizing several power optimization strategies. The system is developed at RTL and verified through simulation before performing synthesis and power analysis [11].

The suggested approach emphasizes lowering chip power while keeping proper system operation.

A. System Overview

The suggested approach is an elevator controller based on FSM that is designed to monitor elevator operations on several floors in a predictable, effective, and safe way.

By continuously comparing the required floor with the present floor position, the controller interprets user floor requests and establishes the direction of travel.

The elevator controller system employs four major inputs, as shown in Fig.1, Global System Clock, Asynchronous Reset, Floor Request (4-bits), and Emergency Stop signal.

The output section controls the motor (Move Up, Move Down, and Motor Stop) along with the indication of the current floor.

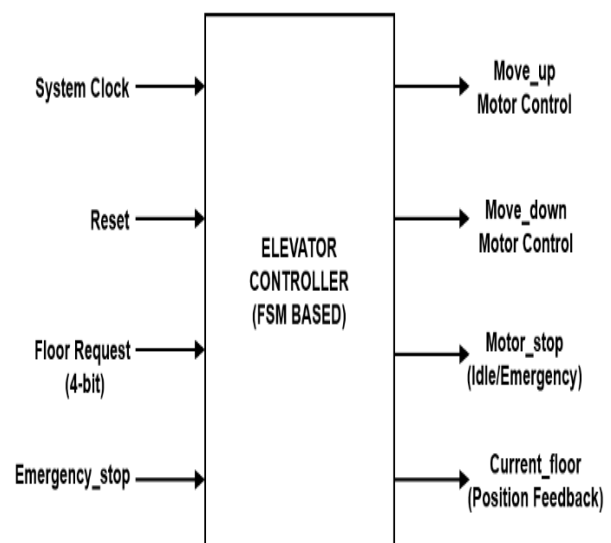


Fig. 1. The elevator controller system architecture.

B. Floor Encoding Scheme

Floor requests are simply shown by using a 4-bit one-hot encoding method. Every floor is given a distinct binary code, guaranteeing for easy decoding and implementation, as displayed in Table I.

This encoding approach simplifies the comparison process by permitting direct plotting between internal control logic and input requests.

TABLE I
FLOOR ENCODING

Floor Number	Encoding
Ground Floor	0001
Floor 1	0010
Floor 2	0100
Floor 3	1000

C. Finite State Machine, FSM Design

Elevator operations are governed by the elevator controller according to floor requests. The system receives floor request signals and determines the appropriate movement of the elevator. The controller is implemented using a FSM with four distinct operational states: IDLE, MOVE_UP, MOVE_DOWN, EMERGENCY. The state transitions depend on: Target Floor (TF), Current Floor (CF) and Emergency stop signal, which is represented in Fig. 2.

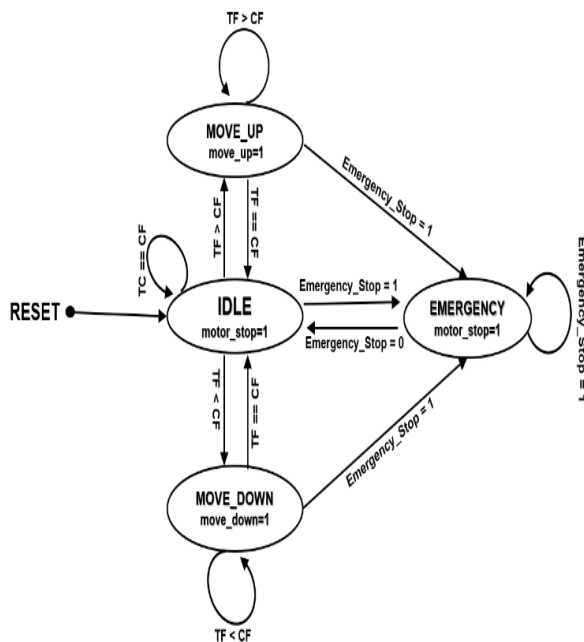


Fig. 2. Finite State Machine, FSM.

D. State Encoding

The FSM states are encoded using a 2-bit binary encoding scheme for efficient hardware implementation, which is shown in Table II.

TABLE II
STATE ENCODING

State	Encoding
IDLE	00
MOVE_UP	01
MOVE_DOWN	10
EMERGENCY	11

The use of parameterized state definitions in Verilog improves readability, scalability, and ease of implementation.

E. Design Flow and Tools Used

The complete design flow follows a standard RTL-to-Gate level implementation methodology [11]. The steps included are shown below Fig. 3.

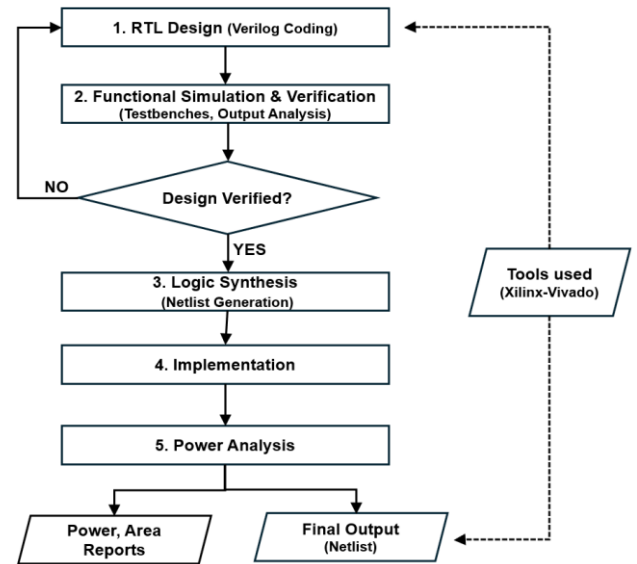


Fig. 3. Flowchart of RTL-to-gate level implementation methodology.

IV. DESIGN WITHOUT LOW POWER OPTIMIZATION TECHNIQUE

The baseline design represents the FSM-based elevator controller implemented without applying any low-power optimization techniques. It serves as a reference for evaluating the proposed design. In this implementation, the state transitions are represented using a 2-bit binary encoding scheme, as shown in Table II.

In binary encoding, multiple bits may change simultaneously between consecutive states, leading to

higher switching activity. In this configuration, the clock signal is continuously applied to all sequential elements, regardless of system activity.

As a result, switching occurs at every clock cycle, even during idle conditions.

Since dynamic power is given by:

$$P_{dynamic} = \alpha C V^2 f \tag{1}$$

Where, α indicates the switching activity factor, C denotes the capacitance, V represents the supply voltage, and f is the operating frequency. The increased switching activity (α) results in higher power consumption [1].

The synthesized schematic shows a direct clock distribution to all modules without any gating or control logic. Since no mechanism is used to suppress unnecessary transitions, the design exhibits higher switching activity and power consumption, highlighting the need for low-power techniques.

The baseline design built without the use of optimization techniques is shown in the reference schematic diagram Fig. 4. The simulation waveform shown in Fig. 5, verifies the correct operation of the baseline elevator controller design under various input conditions.

The power report for baseline design shown in Fig. 6, reveals a total on-chip power consumption of 1.684 W, with dynamic power dominating the power profile by contributing approximately 1.587 W of the total consumption.

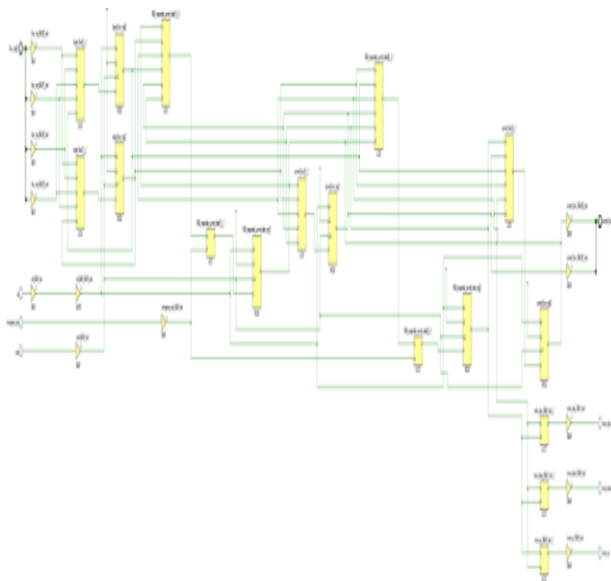


Fig. 4. Schematics without Optimization.

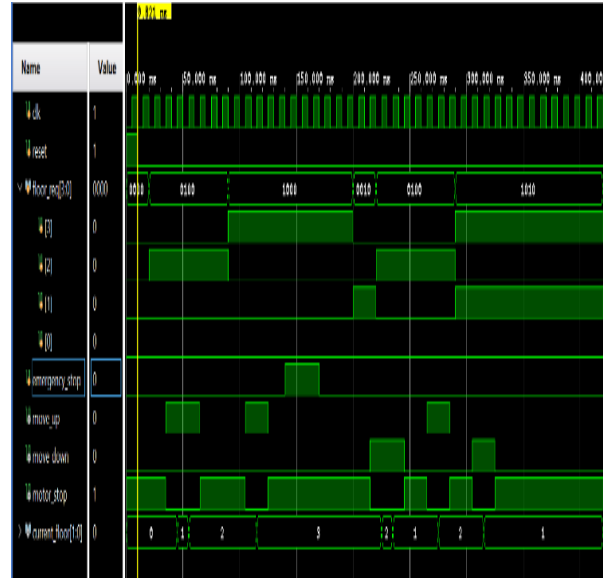


Fig. 5. Waveform without Optimization.

Summary

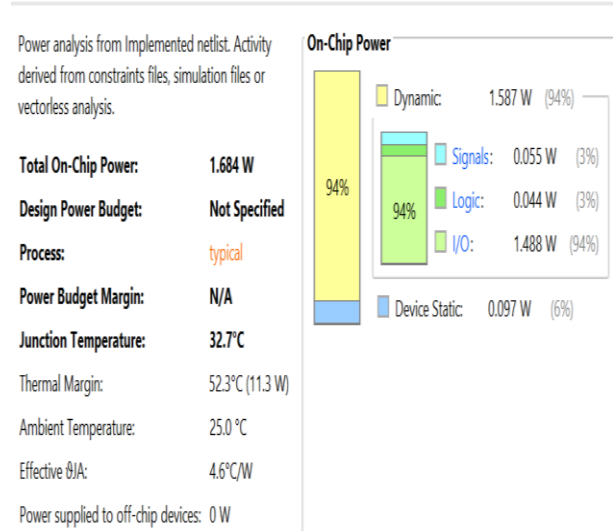


Fig. 6. Power consumption without Optimization.

V. DESIGN WITH POWER-AWARE STATE ENCODING

State encoding significantly affects switching activity in a FSM. In conventional binary encoding, multiple bits may change simultaneously during state transitions, leading to increased switching activity and higher dynamic power consumption [4].

To minimize this effect, Gray code state encoding is used in the proposed design, which is shown in Table III.

TABLE III
STATE ENCODING USING GRAY CODE

State	Encoding
IDLE	00
MOVE_UP	01
MOVE_DOWN	11
EMERGENCY	10

The schematic shown in Fig. 7, shows the elevator controller design after applying state encoding approach.

The simulation waveform using gray encoding, as shown in Fig. 8, demonstrates correct elevator operation with proper floor transitions. Although the external behaviour remains unchanged, Gray encoding ensures one-bit state transitions, reducing switching activity and improving power efficiency. The power analysis of this design is shown in Fig.9, a total on-chip power consumption of 1.582 W, where dynamic power contributes nearly 1.486 W of the overall power.

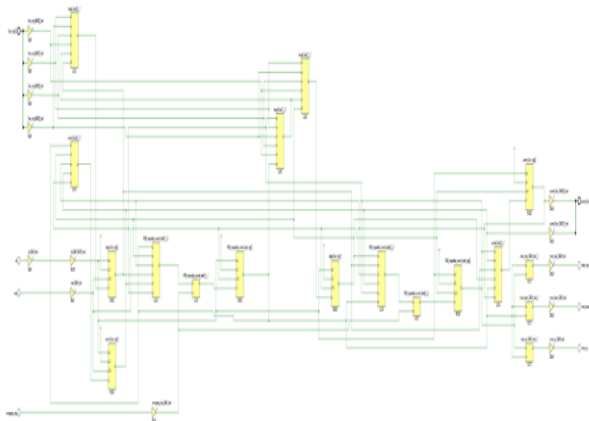


Fig. 7. Schematics diagram of state encoding techniques.

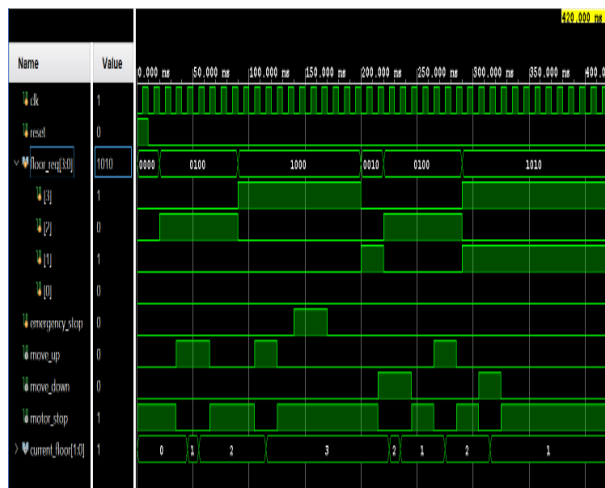


Fig. 8. Simulation waveform of state encoding strategies.

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power: 1.582 W
Design Power Budget: Not Specified
Process: typical
Power Budget Margin: N/A
Junction Temperature: 32.2°C
 Thermal Margin: 52.8°C (11.4 W)
 Ambient Temperature: 25.0 °C
 Effective θ_{JA} : 4.6°C/W
 Power supplied to off-chip devices: 0 W

On-Chip Power

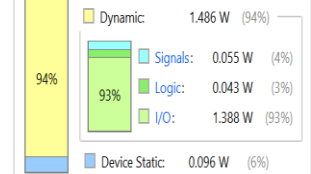


Fig. 9. Power consumption with state encoding techniques.

VI. DESIGN WITH POWER AWARE STATE ENCODING AND CLOCK GATING

Clock gating is an effective method for minimising dynamic power by limiting unnecessary clock-driven switching in sequential circuits. In typical synchronous systems, the clock signal toggles continuously, even when no state updates are required, resulting in avoidable power consumption.

In the proposed design, Gray state encoding and clock gating are implemented to reduce switching activity. The clock enable (clk_en) signal that controls register updates:

- If clk_en = 1 → normal operation
- If clk_en = 0 → registers hold their state (no switching)

From the dynamic power eq.1, it is evident that disabling unnecessary clock activity reduces the switching factor (α), thereby lowering dynamic power.

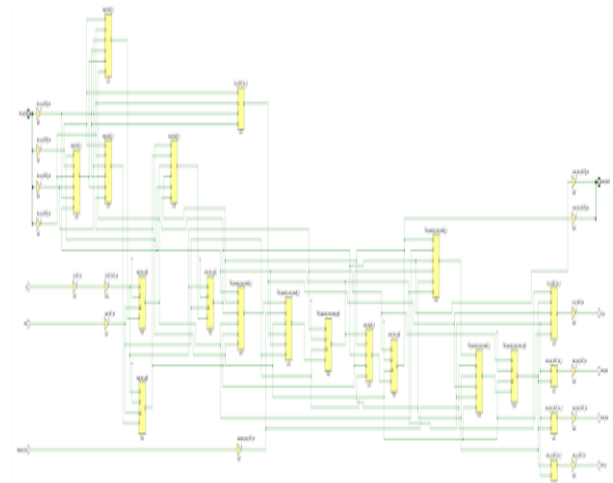


Fig. 10. Schematics with gray encoding techniques and clock gating.

The schematic depicts as shown in Fig. 10, the elevator controller design incorporating gray encoding with clock gating, where clock signals are conditionally propagated to selected registers based on the enable signal, thereby reducing unnecessary switching activity.

The simulation waveform of the elevator controller with Gray encoding and clock gating, as shown in Fig. 11, demonstrates correct functionality with proper floor transitions. It is observed that state updates occur only when `clk_en` is active, thereby reducing unnecessary switching activity and improving dynamic power efficiency.

The power report for this design shown in Fig. 12, the total on-chip power consumption is measured to be 1.062 W, with dynamic power accounting for approximately 0.968 W of the total.

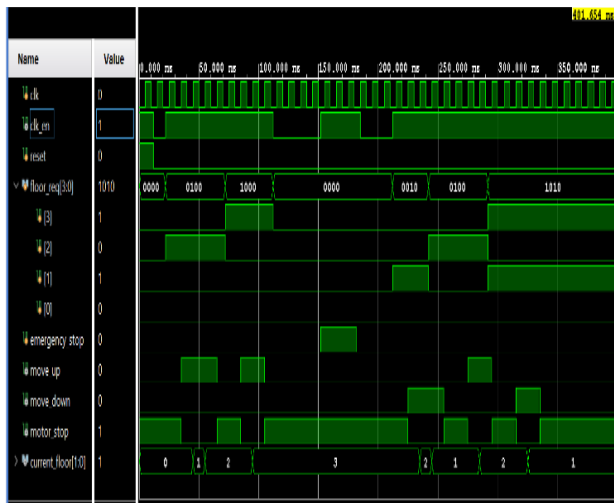


Fig. 11. Waveform with gray encoding techniques and clock gating.

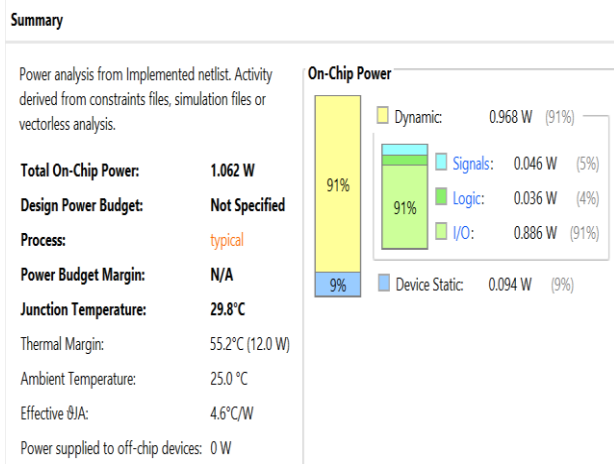


Fig. 12. Power consumption with gray encoding techniques and clock gating.

VII. RESULTS

Result The proposed FSM-based elevator controller was designed and implemented using RTL modeling. After functional verification through simulation, the design was synthesized and analyzed to evaluate its power consumption. Several power optimization techniques were applied sequentially, including power-aware state encoding and state encoding with clock gating.

The results obtained from each stage were compared with the baseline design to analyze the effectiveness of these techniques. Initially, the elevator controller was synthesized without applying any power optimization techniques. The power analysis results show that total on-chip power consumption was 1.684 W. The dynamic power consumption was 1.587 W, consisting of cell internal power and net switching power. The static power of the design was measured as 0.097 W. These results serve as the reference for evaluating the improvements obtained through optimization techniques.

Gray code encoding was used in place of binary encoding to optimize the FSM state encoding. Gray encoding minimizes the transition of bit changes between two states, which reduces the amount of switching activity.

Using the above approach, it resulted in a 6.0 % reduction in total on-chip power, from 1.684 W to 1.582 W. A 6.36 % improvement over the original design was achieved by reducing the total dynamic power from 1.587 W to 1.486 W. The overall power efficiency is improved since there was less switching activity, although a minor drop in static power caused by junction temperature [12]. To maximize power reduction, optimization techniques such as clock gating and power-aware state encoding using gray code were combined. The optimizations gave the best results. The total on-chip power decreased to 1.062 W, resulting in a reduction of 36.69 % and the dynamic power was minimized to 0.968 W, which is 39.0 % less than the initial power. In addition, static power reduced 0.097 to 0.094 W because of the reduced junction temperature [12].

TABLE IV
POWER REDUCTION AFTER APPLYING LOW-POWER DESIGN TECHNIQUES

Configuration	Total on Chip Power (W)	Dynamic power (W)	Static power (W)	Total on-chip power reduction vs. baseline	Dynamic power reduction vs. baseline
Baseline	1.684	1.587	0.097	0 %	0 %
Power-Aware State Encoding	1.582	1.486	0.096	6.05 %	6.36 %

Power-Aware State Encoding + Clock Gating	1.062	0.968	0.094	36.69 %	39.00 %
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VIII. CONCLUSION

The design and implementation of a low-power FSM-based elevator controller through RTL modeling were given in this study. Various power optimization techniques, including power-aware state encoding and power-aware state encoding with clock gating were applied to improve power efficiency. The results demonstrate a considerable reduction in both on-chip power and dynamic power, with improvements of 36.9 % and 39.0 %, respectively, relative to the baseline design. These findings demonstrate that the use of low-power techniques effectively enhances the energy efficiency of digital systems without affecting functionality. The proposed approach can be extended to other FSM-based designs for developing power-efficient VLSI systems.

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