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Energy Efficient ALU Design using Adaptive Clock Gating Techniques for Low-Power VLSI Architectures

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ABSTRACT

The demand to spare energy while creating efficient Very Large Scale Integration (VLSI) systems continues to increase due to the rise in use of portable devices like cell phones that access Internet of Things (IoT). This means that there is a need for designing a low-power computation unit. As a main component of digital processors, Arithmetic Logic Units (ALU) account for a major portion of system power consumption because they operate continuously throughout their operational life cycle. In addition to those reasons, this study proposed an energy efficient ALU as an example of an adaptive clock gating based on reducing switching activity that is not needed, therefore minimizing the amount of dynamic power consumption. The proposed design is developed in Verilog HDL at Register Transfer Level (RTL) and evaluated using standard Electronic Design Automation (EDA) tools via simulation. The fine grained adaptive clock gating concept allows for selective activation of ALU modules where operational requirement dictates. Performance metrics include power, delay, Power Delay Product (PDP), and energy measurements. Based on our results, the proposed adaptive ALU reduces the power from 52.30 µW to 24.10 µW for a 53.92% reduction of power, while the PDP has decreased from 109.83 pJ to 55.43 pJ. The delay increased slightly from 2.10 ns to 2.30 ns, however, the overall energy efficiency increased considerably demonstrating the effectiveness of the proposed solution.

Keywords— Adaptive Clock Gating, Low-Power VLSI Design, Arithmetic Logic Unit (ALU), Power Delay Product (PDP), Energy-Efficient Architectures

I. INTRODUCTION

The rapid expansion of portable electronics, IoT devices, and high-performance computing systems has substantially increased the demand for energy-efficient VLSI design. The ALU, as a core component of digital systems, is responsible for executing arithmetic and logical operations [2]. Since ALUs operate continuously within processors, they contribute substantially to overall power consumption. Therefore, improving the power efficiency of ALUs has become a critical research focus in modern VLSI architectures [3, 4]. In CMOS-based VLSI circuits, power dissipation primarily arises from dynamic switching activity, short-circuit currents, and leakage currents [5]. Dynamic power consumption, due to unnecessary switching of transistors, is the major contributor in synchronous digital circuits. A significant portion of the total system power is often consumed by clock signals driving sequential elements; as these are one of the major sources of switching activity [6]. Traditional ALU designs do not take into account clock distribution management adequately and hence create redundant transitions even if some functional units are idle. This makes it imperative to have advanced techniques for reducing power by controlling clock activity intelligently yet without any degradation in performance [7].

Adaptive clock gating has also become an appealing method to reduce the dynamic power consumption by disabling the clock signal to the inactive parts of a circuit [8]. In comparison to the traditional clock gating techniques, the adaptive clock gating is a dynamic mechanism where the gating conditions are adjusted according to the operational needs in real time [9]. This is to guarantee that the clock signals reach only the required portions of the ALU, and that unnecessary switching activity is further alleviated and the overall energy efficiency enhanced. With the adaptive control logic, the ALU is able to detect idleness, and avoid unnecessary operations hence the power usage is optimized [10] besides saving power, performance and area efficiency are also important design considerations. Adaptive clock gating implementation should have low delay overheads and should not be complex and have a negative effect on circuit timing or silicon area. Hence, there is a trade-off between the power optimization, the speed of a computational unit, and the cost of the hardware when designing an energy-efficient ALU [11]. The adaptive clock gating methods may be further improved with sophisticated

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design techniques such as fine-grained gating and smart control signal generation [12].

Additionally, as semiconductor technology is scaled down to submicron levels, another factor, leakage power, is becoming prominent. Though clock gating is generally used for reducing dynamic power, when it is integrated with other methods such as power gating and multi-threshold CMOS (MTCMOS), it is possible to achieve an efficient energy-saving system [13]. In this regard, it is clear that adaptive clock gating is an essential method for implementing other optimization strategies for achieving low-power VLSI systems [14,15].

The study develops an energy-saving ALU design which implements adaptive clock gating methods that operate efficiently in low-power VLSI systems. The solution intends to eliminate unneeded switching operations while improving power efficiency and sustaining high computational capabilities. The implementation of intelligent gating methods results in better energy savings for the design when compared to traditional ALU design methods. The developments play an essential role in extending battery lifespan for mobile devices while supporting continuous operation of contemporary electronic systems. The following research objectives are presented below:

- To design a baseline Arithmetic Logic Unit (ALU) using conventional CMOS logic for performance comparison
- To develop an energy-efficient ALU architecture using adaptive clock gating techniques
- To reduce dynamic power consumption by minimizing switching activity in ALU modules.
- To analyze the impact of adaptive clock gating on delay, power, and Power Delay Product (PDP).
- To evaluate and compare the performance of conventional, clock-gated, and proposed ALU designs using simulation tools

II. REVIEW OF LITERATURE

The increasing need of VLSI systems that are energy-efficient has prompted massive research on optimization of ALUs which are vital components used in modern processors. There are a number of studies that have discussed the various methods of power reduction, specifically clock gating and dynamic voltage scaling. The research by Hassan et al. (2025) [16] was based on the comparative study of Dynamic Voltage and Frequency Scaling (DVFS), Clock Gating, and a hybrid variant of DVFS and Clock Gating. Their findings showed that although DVFS alone does not offer large amounts of power reduction (2.59%), clock gating can reduce power consumption by almost fifty percent (52.30 µW to 32.28 µW). In addition, the hybrid method yielded up to 54 percent of power reduction and 21 percent-time saving, which contributed to the effectiveness of integrating the multiple methods. On the same note, Hameed et al. (2022) [17] introduced a better signal-based clock gating algorithm with tri-state logic, which reduced dynamic power utilisation in ALU architectures by 24.90%. Vo et al. (2024) [18] also followed this idea by providing a hybrid data-driven clock gating method to RISC-V-based ALUs with a 46.67 percent power cut, but at the cost of a small area overhead. All these studies highlight the fact that clock gating (particularly with adaptive or hybrid techniques) is important in lowering switching activity and enhancing energy efficiency in ALU architectures.

The use of integrated power management structures and architectural-level optimizations has similarly been examined as an energy efficiency mechanism in addition to clock gating. In the study presented by Borde et al. (2025) [19], the authors detail an ALU integrated with a Clock and Power Management Unit (PMC) that integrates several (active, sleep, and deep sleep) modes of operation and switch dynamically between them on an FPGA platform to achieve significant power savings while still maintaining computational throughput, demonstrating workload aware power management. In their research, Surendar et al. (2026) [20] presented an energy-efficient PPA-optimized VLSI architecture incorporating dynamic voltage and frequency scaling (DVFS), micro-gated power gating, and near-threshold operation allowing for large efficiency improvements of 42 percent more performance per Watt and significant reductions in total power consumption with very little area overhead. Antolak et al. (2022) [21] examined the combined effects of frequency scaling and gating techniques for real-time systems, showing that dynamic energy consumption could be reduced without exceeding timing constraints. Zhu et al. (2026) [22] developed a workload aware optimization-enabled ALU that incorporates adaptive clock and power gating techniques in an effort to achieve both large reductions in dynamic and leakage energy and high-throughput, representing only a small fraction of other modern VLSI design methods that employ adaptive, intelligent, and system-level power management techniques

In addition to clock gating and architectural optimization, there has been discussion of alternative design methodology as well so as to further trim down power consumption in ALU and computational units. Vanlalchaka et al. (2023) [23] suggested an adiabatic logic-based ALU design based on MOSFET and FinFET implementation, with a maximum power saving of up to 95.22% with the use of FinFET.

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Likewise, Gate Diffusion Input (GDI) logic was applied in Subbulakshmi et al. (2023) [24], where they have implemented an ALU-based filter bank, which has resulted in drastic power (as little as 91.4) and area (fewer transistors) reductions. Chowdam et al. (2025) [25] investigated approximate computing with clock gating in multiplier design to save up to 18.81% of the power and still obtain an acceptable error tolerance with acceptable accuracy in error-tolerant applications. Another example of power optimization was demonstrated by Mohamed et al. (2021) [26] who showed that integrated clock gating can be used in sequential circuits to save up to 98% of power, based on removing unnecessary clock transitions. Also, Mendez et al. (2024) [27] prioritized the design of computational units to optimize medical image processing, which reduced the Power Delay Product (PDP) by 46.87% and emphasized the significance of efficient designs of arithmetic units. Together, these works prove that clock gating in conjunction with new technologies like adiabatic logic, approximate computing and optimized circuit design can improve the energy efficiency of ALUs and future VLSI systems to a considerably greater degree.

III. RESEARCH METHODOLOGY

This study aims to create and test an ALU that consumes minimal power through its adaptive clock gating design in VLSI systems. The methodology of the project consists of multiple stages that include design specifications as well as implementation and simulation and performance assessment. Fig. 1 depicts the architecture of the proposed methodology.

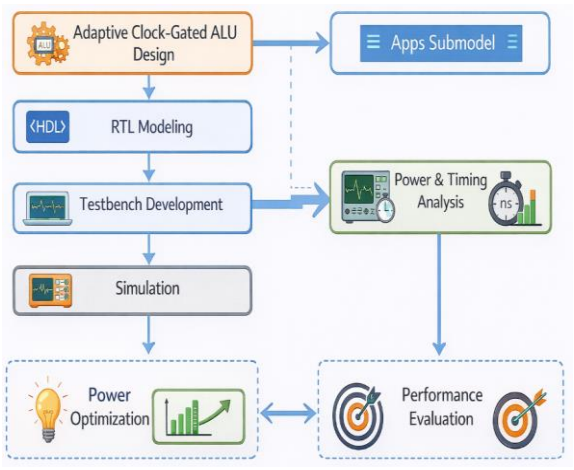

Fig. 1. Proposed Methodology

A. Arithmetic Logic Unit (ALU) Architecture

The ALU is a basic component of digital processors that does arithmetic functions (addition, subtraction, and multiplication) as well as logical functions (AND, OR, NOT, XOR). A baseline ALU is created in this study using regular CMOS logic with no power optimization methods. This design will be used to compare improvements made possible by adaptive clock gating. The ALU consists of:

- Arithmetic unit (adder, subtractor, multiplier)
- Logic unit (AND, OR, XOR, NOT gates)
- Multiplexer (MUX) for selecting operations
- Control unit for operation selection

B. Complementary Metal-Oxide-Semiconductor CMOS Logic and Switching Activity

The baseline ALU is implemented using CMOS technology. In CMOS circuits, power consumption is mainly due to switching activity, short-circuit current, and leakage current.

The total power consumption is given by:

$$P_{total} = P_{dynamic} + P_{short-circuit} + P_{leakage} \quad (1)$$

Where:

$P_{dynamic}$: Power due to switching activity, $P_{short-circuit}$: Power during transistor switching, $P_{leakage}$: Static power due to leakage currents

Dynamic Power Consumption:

In CMOS-based ALUs, dynamic power is the major part because there is a lot of switching. It can be calculated with this formula:

$$P_{dynamic} = \alpha C_L V_{dd}^2 f \quad (2)$$

Where:

α: Switching activity factor, C_L: Load capacitance, V_{dd}: Supply voltage, f: Clock frequency

Propagation Delay:

The performance of the ALU depends on its propagation delay which is based on how fast the transistors switch and how much capacitance they load.

$$t_{pd} = R_{eq} \cdot C_L$$

Where:

R_{eq}: Equivalent resistance of transistors, C_L: Load capacitance

Power Delay Product (PDP):

To evaluate energy efficiency, Power Delay Product (PDP) is used:

$$PDP = P_{average} \times t_{delay} \quad (3)$$

C. Adaptive Clock Gating (ACG) Technique for Power Optimization

ACG is a low-power design method that is applicable to reducing dynamic power consumption in synchronous VLSI circuits, through the selective disabling of the clock signal to idle modules. Traditional design of the ALU also makes the clock

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signal constantly available to all the working units irrespective of activity, unnecessarily switching and dissipating more power. The adaptive clock gating eliminates this shortcoming by dynamically gating the clock, in response to real time operation needs.

Principle of Clock Gating:

Clock gating operates on the principle that the enable signal is added so that the clock can be forwarded to a specific module or not. The gated clock signal is determined as:

$$CLK_{gated} = CLK \cdot Enable \quad (4)$$

Where:

CLK= original clock signal, $Enable$= control signal (1 = active, 0 = idle)

When the module is idle (Enable=0), the clock signal is blocked, preventing unnecessary switching activity.

Adaptive Gating Mechanism:

In adaptive clock gating the enable signal is dynamic and is generated depending upon input activity and type of operation and control signal of the ALU.

Impact on Dynamic Power Consumption:

CMOS-based VLSI circuits have dynamic power consumption as the controlling factor of total power especially in synchronous systems such as ALUs where clock signals provide continuous switching. It is as a result of charging and discharging load capacitances as logic changes occur. This dynamic power is mathematically given as:

$$P_{dynamic} = \alpha C_L V_{dd}^2 f \quad (5)$$

Adaptive clock gating reduces the switching activity factor α, resulting in:

$$\alpha_{eff} = \alpha(1 - G)$$

Where:

G= gating efficiency (fraction of time clock is disabled)

Thus, the modified dynamic power becomes:

$$P_{dynamic}^{gated} = \alpha(1 - G) C_L V_{dd}^2 f$$

This shows that power consumption decreases proportionally with the reduction in switching activity.

Reduction in Clock Power:

Clock networks contribute a significant portion of total power consumption. The power consumed by the clock can be expressed as:

$$P_{clock} = C_{clock} V_{dd}^2 f \quad (6)$$

With clock gating:

$$P_{clock}^{gated} = C_{clock} V_{dd}^2 f (1 - G)$$

Thus, disabling the clock during idle periods significantly reduces overall power consumption.

Design of Gating Logic:

The gating logic is typically implemented using AND gates or integrated clock gating (ICG) cells. A latch-based clock gating approach is often preferred to avoid glitches:

$$CLK_{gated} = CLK \cdot Latch(Enable) \quad (7)$$

This ensures stable clock transitions and avoids spurious switching.

Effect on Performance:

Although clock gating reduces power, it introduces a small delay overhead due to additional gating logic:

$$T_{total} = T_{ALU} + T_{gating}$$

However, with optimized design, this delay is minimal compared to the power savings achieved.

Energy Efficiency Improvement:

Adaptive clock gating helps in improving energy efficiency because it reduces unnecessary transitions in the clock signal. This results in reducing unnecessary charge/discharge of capacitive nodes. This not only helps in reducing power dissipation but also improves system reliability.

$$E = P_{total} \times T_{operation}$$

With adaptive clock gating:

$$E_{gated} = P_{gated} \times T_{operation}$$

Percentage energy saving:

$$\%Energy\ Saving = \frac{E_{normal} - E_{gated}}{E_{normal}} \times 100 \quad (8)$$

D. Proposed ALU with Adaptive Clock Gating Architecture

The proposed ALU architecture includes adaptive clock gating techniques in the traditional ALU design to minimize the dynamic power consumption. As opposed to the traditional design, where a clock signal is always provided to all functional units, in this design, a clock signal is provided to only one of the functional units depending on the required operation. The ALU is made up of an adder and subtractor, a multiplier, (AND, OR, XOR, and NOT) gates, a (MUX), and a control unit. The design adds to each functional block an independent clock gating cell that turns the clock on and off based on the needs of the operation. The control unit produces operation-dependent control signals that are then used to generate enable signals for clock gating.

The gated clock for each module is defined as:

$$CLK_{gated,i} = CLK \cdot Enable_i$$

The enable signal is generated based on the operation code (opcode) and input activity:

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$$Enable_i = f(Opcode, Input\ Activity$$

$$Enable_i = \{1, if\ module\ i\ is\ selected\ 0, otherwise$$

This ensures that only the required functional unit receives the clock signal, while all other units remain inactive, thereby eliminating redundant switching activity.

E. Fine-Grained Clock Gating Strategy

The proposed architecture uses fine-grained clock gating, where clock control is implemented at the level of individual functional modules like adders, multipliers, and logic units instead of gating the whole ALU as one block. This method allows for more accurate regulation of switching activity since only the needed sub-module gets activated for a given operation while all other modules stay idle; thus, achieving more power savings than coarse-grained gating by preventing unnecessary clock transitions at a much lower level.

Theoretically, the fine-grained clock gating is effective when the switching activity factor is minimized in several modules. The best switching activity may be given as:

$$\alpha_{eff} = \sum_{i=1}^{n} \alpha_i \cdot Enable_i \quad (9)$$

where α_i represents the switching activity of the i^{th} module and $Enable_i$ determines whether the module is active.

Accordingly, the total dynamic power consumption of the ALU is given by:

$$P_{dynamic}^{proposed} = \sum_{i=1}^{n} \alpha_i \cdot Enable_i \cdot C_{L,i} \cdot V_{dd}^2 \cdot f \quad (10)$$

This expression demonstrates that power is cut down proportionately by disabling non-operational modules. Moreover, fine-grained gating is also used to restrict the propagation of glitches and minimize inside node transitions, which is more energy efficient. Therefore, this technique is very useful in contemporary low-power VLSI systems where operation depends on workloads.

The proposed energy-efficient adaptive clock gated ALU is designed in Hardware Description Language (HDL) to confirm the correctness of its functionality as well as to test its efficiency in a realistic design setup. It is developed in this study that Verilog HDL is employed to model the baseline ALU as well as the proposed clock-gated ALU architecture at the Register Transfer Level (RTL). It is designed in a modular fashion with each functional unit of the ALU represented as its own module (the adder, subtractor, multiplier and logic unit). The adaption clock gating logic is incorporated into each of the modules by addition of enable controlled clock signals. This is a modular design that enhances scalability, reusability and simplicity of verification.

The gated clock signal for each module is implemented as:

$$CLK_{gated} = CLK \cdot Enable \quad (11)$$

where the Enable signal is produced in accordance to the control unit, through the operation code and input conditions. The RTL modeling is done so that the design is accurate in its representation of data flow and control logic and has synthesis with standard EDA tools.

F. Simulation Setup and Parameters:

Numerous simulation methodologies using well-established industry standard electronic design automation (EDA) tools can be used to verify the effectiveness of the proposed energy saving ALU utilizing adaptive clock gating. The simulations will be executed in an environment set up to evaluate both functional correctness, power consumption, and delay characteristics of both a traditional ALU and the proposed clock gated ALU. The design will be simulated at the RTL level using EDA tools including ModelSim or Vivado. Synthesis and power analysis will be performed by using analytical tools such as Synopsys Design Compiler or Vivado. The design will be simulated in using consistent simulation conditions in order to enable a fair comparison between both traditional and proposed designs. Table 1 provides a summary of the simulation conditions and design parameters utilized during the evaluation of the proposed ALU architecture.

Input Stimulus and Testbench:

To verify all ALU operations, a test bench was developed that incorporated multiple inputs across all combinations of control signals and both active and inactive states. This simulates the performance of adaptive clock gating with respect to reducing switching activity.

Power Analysis Setup:

To analyze the power consumption based on the switching activity during simulation, the total power is represented by:

$$P_{total} = P_{dynamic} + P_{static} \quad (12)$$

where dynamic power depends on switching activity and static power on leakage currents.

Timing Analysis:

The timing performance of the adaptive clock-gated ALU is characterized by propagation delay and critical path delay, both of which represent the total delay for the ALU:

$$T_{total} = T_{logic} + T_{gating}$$

This helps analyze the trade-off between power reduction and delay overhead.

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TABLE I.
SIMULATION PARAMETERS

Parameter	Value	Description
Technology Node	45 nm CMOS	Technology used for implementation
Supply Voltage (V_{dd})	1.0 V	Operating voltage of the circuit
Clock Frequency (f)	100 MHz	System clock frequency
Operating Temperature	25°C	Ambient simulation temperature
Load Capacitance (C_L)	As per synthesis results	Output load capacitance of circuit nodes
Design Language	Verilog HDL	Hardware description language used
Simulation Tool	ModelSim / Xilinx Vivado	Tool used for functional simulation
Synthesis Tool	Synopsys / Vivado	Tool used for synthesis and analysis
Input Test Vectors	Random & predefined	Used for functional verification
Power Analysis Method	Switching activity-based	Based on simulation waveform analysis

G. Performance Evaluation Metrics

The proposed energy-efficient ALU with adaptive clock gating is validated against key performance indicators (KPI's) used to assess power, speed, and overall design optimization. All of these KPI's provide a global perspective on how successful the improvements made in the new method of designing an ALU compare to traditional methods.

Propagation Delay - The propagation delay defines how fast an ALU operates. Propagation Delay is defined as:

$$t_{delay} = R_{eq} \cdot C_L \quad (13)$$

Power Delay Product (PDP) represents the energy efficiency of the circuit:

$$PDP = P_{average} \times t_{delay}$$

Energy per operation is calculated as:

$$E = P_{total} \times T_{operation}$$

Area is measured in terms of logic resources such as gates or LUTs. The total area is given by:

$$A_{total} = A_{ALU} + A_{gating}$$

To evaluate improvement:

$$\%\ Power\ Reduction = \frac{P_{baseline} - P_{proposed}}{P_{baseline}} \times 100$$

IV. RESULTS AND DISCUSSION

This section discusses the results of testing the Adaptive Clock Gated ALU, and compares them to the traditional designs based upon key performance indicators including Power, Delay, PDP, and Energy Consumption, and highlights that considerable improvements were gained when compared to traditional methods of designing ALUs.

Table 2 presents a comparative analysis of conventional, clock-gated, and proposed adaptive ALU designs based on key performance metrics. The design shows its power consumption and PDP reduction capabilities which result from the developed system design while its delay and area requirements increase only a little. The results show that the system achieves better energy efficiency together with improved operational performance.

TABLE II:
PERFORMANCE COMPARISON OF CONVENTIONAL, CLOCK-GATED, AND PROPOSED ALU DESIGNS

Parameter	Conventional ALU	Clock Gated ALU	Proposed Adaptive ALU
Power (µW)	52.30	32.28	24.10
Delay (ns)	2.10	2.25	2.30
PDP (pJ)	109.83	72.63	55.43
Area (LUTs/Gates)	100%	105%	108%
Power Reduction (%)	—	38.28%	53.92%

Fig. 2 displays the power consumption comparison of three ALU designs; standard ALU, clock-gated ALU, and suggested adaptive ALU. The traditional ALU has the greatest power consumption of 52.3 uW and the clock-gated ALU has a power consumption of 32.28 uW, which is a great improvement. The adaptive ALU suggested has the lowest power consumption of 24.1 µW, which confirms that it is more efficient. Generally, the findings show that clock gating and adaptive clock gating reduces the residual value by a significant amount of about 38.28 and 53.92 percent respectively relative to the traditional design.

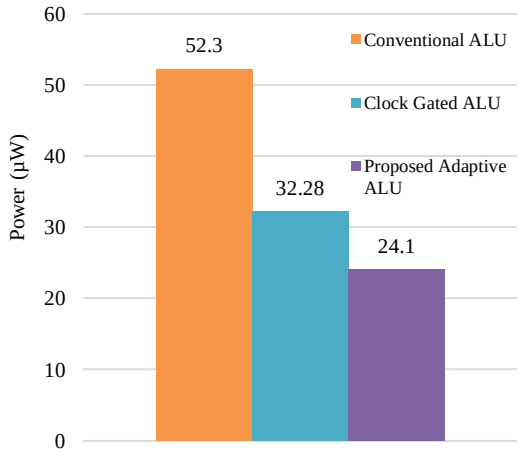

Fig. 2. Power consumption comparison of ALU designs

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The fig. 3 gives a comparison of the propagation delay of conventional, clock-gated and proposed adaptive ALU designs. The traditional ALU has delay of minimum feasible 2.1 ns and clock-gated ALU have a small higher delay of 2.25 ns because of the introduction of some gating logic. The maximum delay of 2.3 ns is recorded in the proposed adaptive ALU, which is slightly higher than the previous one. Although this slightly increases the overhead, the gain is within reasonable limits, which proves that the offered design is performance-efficient and at the same time able to reduce power substantially.

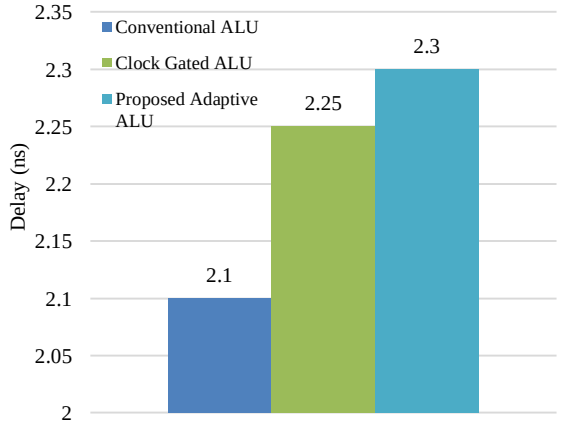

Fig. 3. Delay comparison of ALU designs

The fig. 4 shows the comparison of PDP of conventional, clock-gated and proposed adaptive ALU design. The traditional ALU has the worst PDP of 109.83 pJ, which shows that it consumes more energy per operation. The ALU clock-gated version makes the PDP 72.63 pJ, which is more efficient. The adaptive ALU proposed has the lowest PDP of 55.43 pJ, which represents a tremendously high amount of energy efficiency improvement. This significant decrease validates that adaptive clock gating is an effective way of reducing the total amount of energy used but still have a fair level of performance.

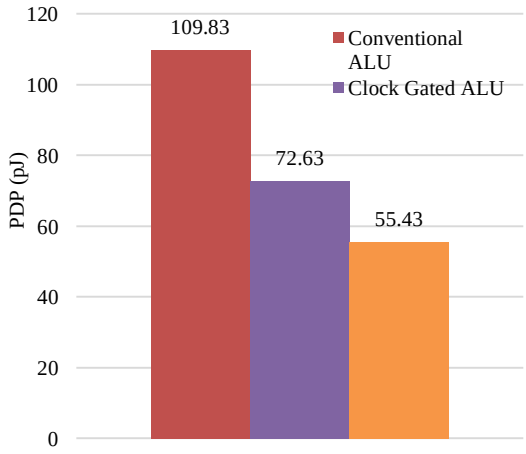

Fig. 4. PDP comparison of ALU designs

Table 3 and the fig. 5 provide a close comparison of power consumption elements between the proposed adaptive ALU designs and baseline designs. The baseline ALU has a greater dynamic power of 45.00 µW, which is greatly lower in the proposed design to 18.50 µW. Equally, the difference between the initial and final values of the static power is -7.30 µW to -5.60 µW and clock power is -20.00 µW to -8.20 µW. Consequently, the overall power consumption reduces to 24.10 instead of 52.30 µW in the proposed ALU and the baseline ALU, respectively. These reductions have been proven through the figure which depicts significant changes in the various components. The proposed design shows almost 53.92 percent reduction in total power, which proves the efficacy of adaptive clock gating.

TABLE III:
POWER CONSUMPTION BREAKDOWN OF BASELINE AND PROPOSED ALU

Component	Baseline (µW)	Proposed (µW)
Dynamic Power	45.00	18.50
Static Power	7.30	5.60
Clock Power	20.00	8.20
Total Power	52.30	24.10

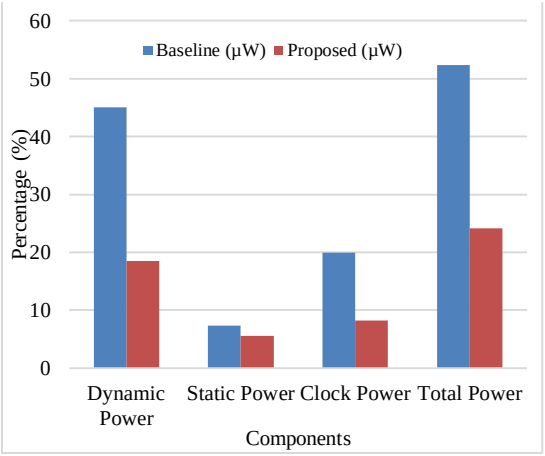

Fig. 5. Power consumption breakdown of baseline and proposed ALU designs

The table 4 and fig. 6 show how switching activity is reduced (α) across different modules of the ALU using adaptive clock gating. From the baseline design, it is evident that the highest switching activity is observed in the multiplier and adder modules at 0.90 and 0.85, respectively. However, these are reduced to 0.45 and 0.42 in the proposed design, indicating a reduction of 50.00% and 50.58%, respectively. Similarly, a reduction is observed in the subtractor module from 0.80 to 0.40 (50.00%), and the highest reduction is observed in the logic unit from 0.75 to 0.30 (60.00%), and in the MUX &

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control module from 0.60 to 0.35 (41.67%). It is evident that adaptive clock gating minimizes switching activity across all modules of the ALU.

TABLE IV:
REDUCTION IN SWITCHING ACTIVITY ACROSS ALU MODULES

Module	Baseline α	Proposed α (with gating)	Reduction (%)
Adder	0.85	0.42	50.58%
Subtractor	0.80	0.40	50.00%
Multiplier	0.90	0.45	50.00%
Logic Unit	0.75	0.30	60.00%
MUX & Control	0.60	0.35	41.67%

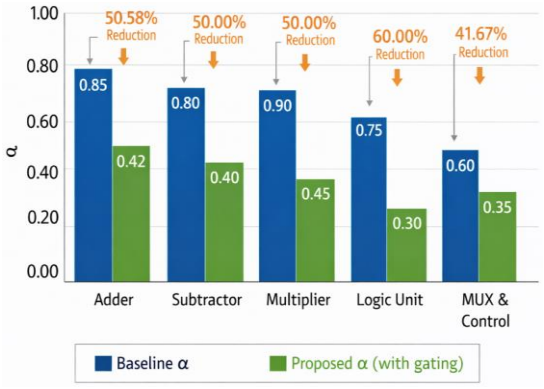

Fig. 6. Switching activity reduction across ALU modules using adaptive clock gating

The table 5 and fig. 7 show the comparison results for energy consumption in conventional, clock-gated, and proposed adaptive ALU designs. The results show that the conventional ALU has the maximum energy consumption at 120.50 pJ. The clock-gated ALU design reduces the energy consumption to 78.20 pJ, which reflects a reduction of 35.10%. The proposed adaptive ALU design reduces the energy consumption to 58.40 pJ, which reflects a significant reduction of 51.53% compared to the conventional design. The graph shows the decreasing trend in energy consumption in all the designs. This shows that adaptive clock gating minimizes the energy consumption, thus improving the energy efficiency of the ALU design.

TABLE V:
ENERGY CONSUMPTION COMPARISON OF ALU DESIGNS

Design	Energy (pJ)	Energy Reduction (%)
Conventional ALU	120.50	—
Clock Gated ALU	78.20	35.10%
Proposed Adaptive ALU	58.40	51.53%

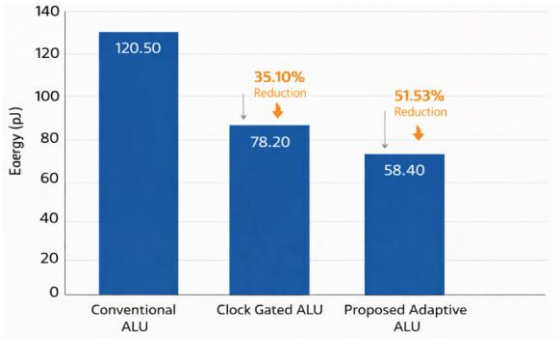

Fig. 7. Energy consumption comparison of ALU designs

V. CONCLUSION AND FUTURE SCOPE

This paper presents the design and analysis of an energy efficient Arithmetic Logic Unit (ALU) using adaptive clock gating techniques for low-power VLSI architectures. The proposed approach effectively reduces unnecessary switching activity by dynamically enabling clock signals only to active functional units. A baseline ALU and the proposed adaptive clock gated ALU is implemented using Verilog HDL and evaluated through simulation using standard EDA tools. The measurements taken shows an improvement in power efficiency, with total power usage decreased from 52.30 µW to 24.10 µW for an overall savings of 53.92%. In addition, the Power Delay Product (PDP) has been reduced from 109.83 pJ to 55.43 pJ, meaning that energy efficiency has been improved. A slight increase in delay from 2.10 ns to 2.30 ns due to the gating overhead is observed, however this is acceptable trade-off for low power implementations. The reduction in switching activity across the ALU modules further substantiates the effectiveness of the proposed technique. Overall, the proposed adaptive clock gating based ALU provides the optimal balance of power, performance and area, making it suitable for modern day low power and high-performance VLSI systems.

Future work will include combining adaptive clock gating with other advanced technologies like power gating and DVFS to obtain greater power savings. The proposed design could also be expanded to larger bit-width ALUs, as well as for use in real time processor architectures to improve overall scalability and performance.

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