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Neuromorphic Computing and Futuristic Processor

Aryan Gautam, Mansi Maurya, Sakshi Singh, Shruti Awasthi

Department of Electronics and Communication,
Gautam Buddha University, Greater Noida, Uttar Pradesh, India.
Corresponding Author: gautamaryan504@gmail.com

ABSTRACT

Neuromorphic computing moves away from the Von Neumann architecture. Instead of developing computers with traditional architecture, neuromorphic computing imitates how the brain could potentially operate by incorporating the construction of neurons and synapses. This can be attributed to the impasses of Moore's Law, the "memory wall," and the demands of traditional computer architecture. This review paper delves into the evolution of computers from their conception to current artificial intelligences and the limits of traditional computers, particularly the "Von Neumann bottleneck." The review demonstrated the differences between basic biology and artificial constructs of neurons. This was used to show how neuromorphic computing and the incorporation of Spiking Neural Networks (SNNs) operate with long-term energy efficiency and large-scale parallelism. Architectures mimicking the brain with synaptic plasticity were termed the "Silicon Brain." This review also encompassed contemporary neuromorphic computing architectures such as Loihi and Loihi 2, TrueNorth, and SpiNNaker2, in addition to memristor technology. This review also elaborated on the various applications of neuromorphic computing in autonomous vehicles, cyber security, Edge AI, and neuromorphic computing's application in healthcare, while also addressing the barriers of use, such as the difficulties of programming and maintaining accuracy in computations. It was concluded that neuromorphic computing holds the greatest potential for the future of energy-efficient computing.

Keywords: Neuromorphic Engineering, Spiking Neural Networks (SNN), Von Neumann Bottleneck, CMOS, Silicon Brain, Edge AI, Event-driven processing, Loihi, Loihi 2, TrueNorth, SpiNNaker2, Memristor, Spike-Timing-Dependent Plasticity (STDP), In-Memory Computing.

I. INTRODUCTION

Neuromorphic computing, also known as neuromorphic engineering, is a discipline that includes the use of very-large-scale systems integrating electronic analog circuits designed to replicate the neurobiological systems of the nervous system. Its goal is to create hardware and software that replicate the structures and functions of the brain's neurons and synapses. Although the field began in the late 1980s, thanks in part to Misha Mahowald and Carver Mead's project of the first silicon retina, it has developed rapidly in recent years to become a possible solution to the limitations of scaling AI. Because most ontological models of deep learning tend to require large data centers, neuromorphic computing is seen as a solution to provide the efficiency needed to develop artificial superintelligence [1].

An important motivation for developing neuromorphic computing is the energy efficiency gap between biological and artificial computing systems. The human brain is very energy efficient, consuming around 20 watts, and is much more powerful than the most powerful computers at pattern recognition, processing senses, and learning. On the other hand, deep learning models of large size are very energy inefficient, consuming hundreds of megawatt-hours, and there's no evidence that this trend can be sustained [2]. To solve the problem of the energy efficiency gap, the big inspiration of neuromorphic engineering is the brain's system of a large number of parallel and event-driven processes. Since this field of study is highly interdisciplinary, integrating many disciplines such as neuroscience, materials science, and computing, it is one of the most rapidly developing frontiers of computing research [3].

II. THE EVOLUTION OF COMPUTING

Computing technology can be segmented into five generations:

- ***First Generation (1940–1956):*** Use of vacuum tubes and magnetic drums. These machines (e.g. ENIAC) were huge, expensive, and generated lots of heat.
- ***Second Generation (1956–1963):*** Use of transistors. Smaller, faster, and more efficient machines.
- ***Third Generation (1964–1971):*** It became possible to integrate huge numbers of transistors in a single silicon chip and to construct heat-manageable computers.
- **Fourth Generation (1971–Today):** The era of Microprocessors (Large Scale and Very Large Scale Integration) where thousands of Integrated Circuits (ICs) are housed on a single chip, leading to the first Personal Computers.
- **Fifth Generation (Today):** In AI, parallel processing, and quantum systems, neuromorphic computing is where we see the greatest growth as we move from calculating to perceiving [9].

Advances in computing generation are increasingly tied to the physical and economic limits of the previous

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generation. Transitioning to neuromorphic systems is tied to the limits of CMOS scaling and the power-limited AI-intensive systems. When the limits of transistor size are reached, computer architects will need to find new paradigms rather than refine the current systems [15].

III. TRADITIONAL ARCHITECTURE AND THE "VON NEUMANN WALL"

The design framework developed in 1945 for the standard von Neumann architecture has been a fundamental tool for developing most computers in existence today. Central Processing Units and memory units are connected to each other by a communications bus.

The Bottleneck: Data and instructions must be "fetched" from memory to the CPU for each operation. As the speed gap between CPUs and memory and bus systems began to widen, these systems caused a bottleneck to efficiency, wasting time and energy.

The Power Wall: Traditional CPUs have a constant power draw because most of them are "always on", even when they are not processing data. This is the source of the recent heat and battery problems in modern smartphones and laptops.

The Von Neumann bottleneck is further compounded by the widening gap between processor speeds and memory access latencies, known as the memory wall. For example, high-performance CPUs can execute instructions within a few picoseconds, whereas main memory access latencies are in the range of tens or hundreds of nanoseconds. This causes CPUs to spend a considerable amount of time idle while waiting for data. These limitations are major challenges of traditional computing and are among the main reasons for the rapid development of neuromorphic computing architectures, of which in-memory computing systems are a promising variant [3].

IV. BIOLOGICAL VS. ARTIFICIAL NEURAL PARADIGMS

The core of neuromorphic engineering is the imitation of the biological neuron, which differs significantly from traditional AI.

Biological Neuron: Neuromorphic engineering revolves mostly around the imitation of biological neurons, leading to a clear divergence from traditional AI. Biological neurons operate through electrochemical impulses, often referred to as "spikes." They operate in parallel and are highly power-efficient, consuming around 20 watts while even outperforming supercomputers in pattern recognition tasks.

Artificial Neuron (ANN): In traditional AI, neural networks use mathematical abstractions in which neurons are represented as floating-point numbers. This approach relies on clock-driven, synchronous processing, which is computationally expensive and demands significant computational resources.

The use of floating-point numbers to represent neurons also reflects a different method of information encoding. In biological systems, neurons represent information through the timing and order of electrical spikes. This principle is used in Spiking Neural Networks (SNNs). In contrast, traditional ANNs use floating-point numbers in their layers, not fully exploiting the event-driven efficiency of biological systems.

The four main models of spiking neurons used in neuromorphic chips are the Hodgkin–Huxley model, the Izhikevich model, the Integrate-and-Fire model, and the Spike Response Model. Among these, the HH model is the most accurate and widely used for biological simulations, whereas the LIF model is the most commonly used because it is the most computationally efficient [8].

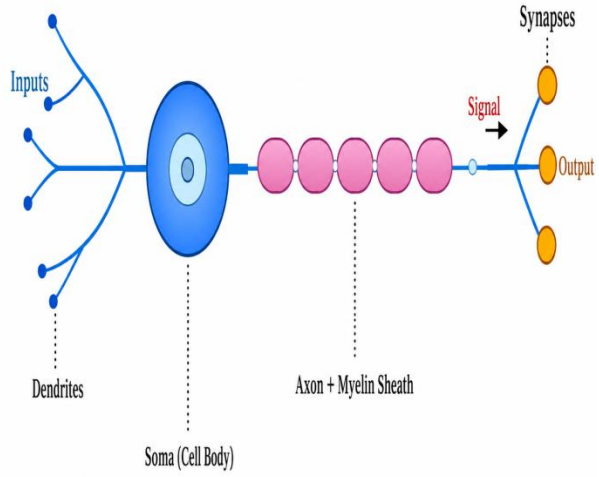

Fig. 1. A Biological Neuron — the first electrically excitable unit of the brain or nervous system that helps in receiving, processing, and transmitting information using electrical and chemical signals [18].

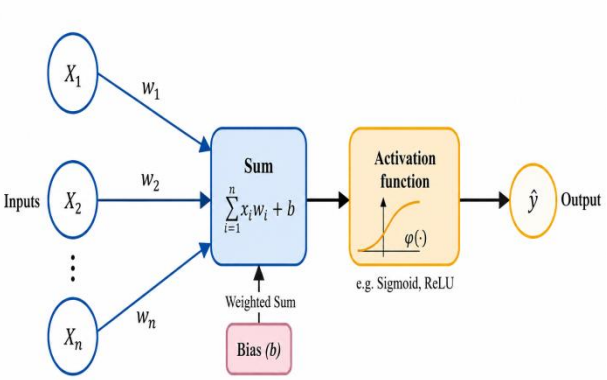

Fig. 2. An Artificial Neuron — a mathematically designed functions that imitates the basic operations of a biological neuron [19].

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V. THE ARCHITECTURE OF THE "SILICON BRAIN"

Neuromorphic architectures, which are non-Von Neumann, consist of three key elements:

- **Artificial Neurons:** These are the computational nodes that, similar to the Integrate-and-Fire model, only communicate when they reach a certain threshold.
- **Synapses:** The connections that link the neurons. In neuromorphic hardware, these are the storage elements of the architecture. Because memory is stored in the synapses, the delay that data travel incurs is eliminated (In-Memory Computing).
- ***Spiking*** Neural Networks: Differing from conventional AI, SNNs have the timing of the spikes carry the information. Because of the "event-driven" nature of SNNs, these systems do not consume power when there is no data to be processed [2].

Another important feature that adds to the flexibility of these systems is Spike-Timing-Dependent Plasticity (STDP). STDP is a learning rule, inspired by biological learning, which adjusts the strength of a synapse by the timing of spikes in pre- and post-synaptic neurons. When the pre-synaptic neuron fires before the post-synaptic neuron in a short time frame, the synapse is strengthened (Long-Term Potentiation). When the order occurs in the inverse way, the synapse is weakened (Long-Term Depression). Because of the simplicity of its design, it is ideal for edge AI, as there are no requirements for labeled data or back-propagation in the learning process (on-chip learning) [6].

SNNs utilize two complementary strategies of rate and temporal coding. Rate coding determines the value by the frequency of the spikes, while in temporal coding, the specific timing of spikes is used to convey the information. Temporal coding is more efficient, as it allows larger values to be expressed with fewer spikes and a lower rate, substantially reducing switching activity and power consumption [8].

A. Emerging Device Technologies: Memristors

Memristor technology, originally hypothesized by Leon Chua in 1971, and now developed with two-terminal devices, is well suited for large-scale deployment of hardware-based neuromorphic synapses. Memristors behave as biological synapses; their synaptic weights (and therefore their resistance) can be set and retained without power, allowing for non-volatile in-memory computation [13].

Functional materials in memristors include HfO2 and TaOx (metal oxides used for RRAM), phase-change materials (PCM), and ferroelectrics like hafnium-oxide-based compounds used in ferroelectric tunnel junctions. RRAM and ferroelectric memristors can consume energy for synaptic operation below the biological neuron threshold of 10 fJ. The lowest reported power consumption of memristive devices, at 4.28 aJ, was used in HfAlOx-based RRAM [13],[14].

Next-generation two-dimensional (2D) materials such as MoS2, In2Se3, and MoTe2 are being explored for their memristive properties. These materials offer exceptional mechanical flexibility, atomic thickness, and tunable electrical properties, making them suitable for high-density integration of flexible electronics and neuromorphic systems [16].

Though the future of memristive hardware is bright, issues such as device-to-device variability and low endurance will negatively impact performance in some applications. New studies suggest using layer ensemble averaging and similar fault-tolerant algorithms to convert hardware variability from a liability to a statistical asset, strengthening inference on arrays with high defect rates [17].

VI. HARDWARE IMPLEMENTATIONS

Many "futuristic processors" have been created to achieve the neuromorphic dream, from individual research chips to massive systems with billions of neurons.

IBM TrueNorth: Has 1 million programmable neurons and 256 million programmable synapses, consuming only 70 milliwatts. In 2014, it demonstrated unmatched energy efficiency for large-scale pattern recognition [5].

Intel Loihi: A many-core processor with on-chip learning, enabling the system to learn and adapt autonomously in real-time with no dependency on the cloud. Loihi established many of the first benchmarks of neuromorphic efficiency for tasks such as constraint satisfaction, graph search, and robot control [4].

Intel Loihi 2: Released in 2021 and built on the Intel 4 process node, Loihi 2 demonstrates a 10x gain in spike computation efficiency, supports 1 million neurons and 120 million synapses per chip, and introduces a fully programmable neuron model and custom instruction set. It supports graded spike payloads of up to 32 bits and is supported by the open-source Lava software framework [11].

Intel Hala Point: Announced in 2024 and deployed at Sandia National Laboratories, Hala Point is the largest neuromorphic system in the world. It includes 1,152 Loihi 2 processors, supports 1.15 billion neurons and 128 billion synapses, and has 140,544 processing cores. With a power consumption of 2,600 W, it achieves 15 TOPS/W for deep neural network processing — 50x faster and 100x more efficient than traditional CPU/GPU systems [12].

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SpiNNaker2: Created at the University of Manchester, SpiNNaker2 has modular and scalable architecture housing over 69,000 interconnected microchips and over 10 billion neurons. Each microchip has 152 ARM cores and it offers over ten times greater efficiency than its predecessor, supporting hybrid SNN/ANN networks [6].

Tianjic: Developed at Tsinghua University, Tianjic is a hybrid platform supporting both spiking neural networks and artificial neural networks. Its hybrid nature makes it one of the most comprehensive and flexible neuromorphic systems [9].

VII. LEARNING ALGORITHMS FOR NEUROMORPHIC SYSTEMS

Developing learning algorithms for neuromorphic systems presents several challenges. The discrete, event-driven paradigm of spiking networks differs from the continuous networks of ANNs that utilize backpropagation. SNNs therefore require different training methods.

- **Spike-Timing-Dependent Plasticity (STDP):** A biologically inspired, unsupervised learning paradigm in which the strength of a connection is modified based on the timing of pre- and post-synaptic spikes. STDP is the primary learning rule for SNNs and, because of its on-chip learning capability, is particularly suitable for edge devices [6].
- ***Surrogate Gradient Methods:*** Since backpropagation cannot be directly applied to SNNs due to the discontinuity of the spike generation function, a smooth approximation of the spike function is used. This enables SNNs to be trained as deep networks and perform complex tasks, and is one of the most active research areas in SNNs [8].
- **ANN-to-SNN Conversion:** This approach first trains a suitable ANN, then converts it into an SNN by transferring the learned weights. While this bypasses many challenges of training SNNs, it often results in a performance drop and may require many time steps to achieve reasonable performance, increasing latency [10].
- ***Hebbian and Reward-Modulated Learning:*** Hebbian learning is based on the principle that "neurons that fire together wire together." Reward-modulated variants employ a global reward signal to guide the learning process, making them suitable for a variety of reinforcement learning applications [8].

VIII. REAL-WORLD APPLICATIONS

A. ***Peripheral Sensing In Autonomous Vehicles:*** the integration of real-time spatial reasoning creates a demand for near-instantaneous visual data processing in autonomous driving systems. Neuromorphic chips significantly reduce energy consumption during data processing, as they require less computation to process "visual spikes" generated by event-based cameras. Collision avoidance systems can react to threats more quickly using event-based processing than conventional frame-based cameras processed by standard cpus or gpus [5].

B. ***Continuous Sensing in Edge AI:*** continuous sensing systems can remain idle for extended periods while still responding to environmental stimuli when "awakened." the event-driven nature of snns enables always-on sensing with near-zero idle power consumption [2].

C. Smart Firewalls: anomaly detection systems can employ neuromorphic chips to mimic biological immunity, providing significantly faster intrusion detection than conventional software firewalls. Snns' temporal processing capability enables detection of time-correlated anomalies that are difficult to identify Using conventional block-processing methods [3].

D. ***Health and Brain/Computer Interfaces:*** There has been a significant increase in research involving neuromorphic algorithms for implantable brain/computer interfaces (bcis). The low-power consumption and real-time characteristics of snns are essential for devices implanted within the human body. Applications include retinal prostheses, cochlear implants, brain interfaces, and neural stimulators used in the treatment of parkinson's disease [6].

E. ***Telecommunications:*** Ericsson research has highlighted the advantages of intel's loihi 2 neuromorphic chip for developing telecom infrastructure. Telecom operators can execute ai workloads on neuromorphic hardware with improved energy efficiency during network optimization processes [12].

F. ***Robotics and Sensory Processing:*** A research team from the national university of singapore developed a robotic system integrating an artificial brain based on loihi along with artificial skin and vision, enabling adaptive, low-power interaction with its environment [4].

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IX. CHALLENGES AND OPEN PROBLEMS

A. ***Scalability:*** Scaling large networks across distributed neuromorphic hardware requires new approaches for spike communication, memory management, computation, and energy efficiency. As the number of transmitted spikes increases over longer distances, communication overhead grows. Scaling to billions of neurons on a single chip would require routing millions of spikes efficiently [8].

B. **Programming Complexity:** Most engineers are familiar with PyTorch or TensorFlow. Programming neuromorphic chips is radically different. Software frameworks such as Intel's Lava, PyNN, Brian2, and Nengo are still in their infancy compared to mainstream AI frameworks [11].

C. ***Accuracy Gaps:*** Neuromorphic systems are particularly powerful for sparse, event-driven workloads. For feedforward network models, achieving a comparable level of accuracy remains problematic. The accuracy gap is smaller due to surrogate gradient and ANN-to-SNN conversion, but more research is still required [10].

D. ***Device Variability in Emerging Hardware:*** The use of memristors and other analog neuromorphic devices suffers from reliability issues due to cycle-to-cycle and device-to-device variabilities. Research is being conducted on robust hardware-algorithm co-design frameworks that tolerate or leverage these variabilities [17].

E. ***Standardization and Benchmarking:*** Frameworks that allow fair comparison of different neuromorphic systems are not yet available. The development of common benchmarks is critical for the improvement of neuromorphic systems and for subsequent industrial investments [7].

X. CONCLUSION

Neuromorphic computing is crossing the boundary are akin to sensory co-processors — excelling at tasks that are sparse, event-driven, and temporally between the calculative and the perceptive. Regular CPUs excel at logic and arithmetic at a high degree of precision and thus remain vital. However, neuromorphic systems structured. By integrating memory and processing, these systems bypass the Von Neumann bottleneck, making a much more sustainable hardware future possible.

The first generation of neuromorphic hardware is now becoming a commercial reality. Research chips such as IBM's TrueNorth opened the way to large-scale systems such as Intel's 1.15-billion-neuron Hala Point. These systems have been integrated with new device technologies such as memristors and 2D materials. From a research perspective, the gap between SNNs and deep learning has been narrowed through new learning techniques based on surrogate gradients and on-chip STDP.

A combination of new device technologies will allow faster integration of neuromorphic systems, with easier-to-use programming systems and established benchmarks. New hardware will integrate algorithms at the design stage to account for the imperfections of the devices. These systems will allow a new generation of intelligent computing that is biologically comparable and will operate at much higher levels of efficiency and performance [15].

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