AOI: 10.100.234513.0290
13th international conference on Microelectronics, Circuits and Systems, Micro2026

Analytical Comparision of Design Parameters in 6T and 10T SRAM Architectures and Memory Array

G. L. Madhumati, Mandala Sai Venkatesh, Manthena Divakar, Konka Bala Murali

Department of Electronics and Communication Engineering
Siddhartha Academy of Higher Education Vijayawada. Andhra Pradesh, 520007, India
Corresponding Author: mandalavenkatesh88@gmail.com

ABSTRACT

This paper presents the design and analysis of 6T and 10T SRAM cells using Cadence Virtuoso at 180nm technology node. Schematic and post-layout simulations are carried out to evaluate power consumption, speed, and area. The proposed 6T SRAM cell achieves a dynamic power of 11.5 µW, leakage power of 120nW, read delay of 0.75ns, and write delay of 0.55ns with an area of 18 µm2. The 10T SRAM cell offers improved read stability with a read delay of 0.475ns and dynamic power of 6.5 µW. Compared to existing works, the proposed design achieves an average power of 11.62 µW against 898,300 W, a reduction of over 99.99%, and a write delay of 0.55ns against 0.67ns, an improvement of 17.9%. The results demonstrate that the proposed SRAM cells are highly efficient for low-power embedded applications. Write Delay: 0.55 ns (proposed) vs 0.67 ns (existing) → 17.9% faster. Average Power: 11.62 µW (proposed) vs 898,300 µW (existing) →99.99%, less power.

Keywords: Area efficiency, CMOS technology, Delay analysis, Low power design, Read stability, SRAM, 6T SRAM, 10T SRAM, 45 nm technology, 180 nm technology.

I. INTRODUCTION

In modern System on Chip (SoC) designs, SRAM occupies the majority of the silicon area, to make our devices more energy-efficient; we have to focus on reducing the power used by the memory. The most effective approach is to use “near-threshold” voltage designs, but this is where the standard 6T SRAM cell hits a wall. Its stability or Static Noise Margin is tied directly to the supply voltage; the transistors are forced to balance being strong enough for a “write” operation while remaining stables enough for a “read.” To overcome these challenges, various alternative SRAM architectures have been proposed [1]. The rest of this paper is organized as follows: In Section II discusses about the problem statement and section III describes system goals, In Section IV literature review on the related topic is presented, In section V describes about the SRAM architectures In section VI describes the proposed hardware architecture and the implementation details, In section VII deals with experimental results and analysis, section VIII covers the conclusions and section IX deals with future scope.

II. PROBLEM STATEMENT

Because of its small silicon area and straightforward design, the traditional 6T SRAM cell is preferred. However, these cells often suffer from read disturbance and high leakage power in low-power modes when forced to operate at lower voltages [2]. The main reason for this is that modern, energy-efficient chips cannot realy on the same transistors to perform both reading and writing. To resolve this, the 10T SRAM architecture was created. By using extra transistors to separate the read and write operations, it significantly increases stability and allows the device to operate at much lower voltages without failing [1], [3]. However, this method increases the size and complexity of the cell’s design. This study compares 6T and 10T architectures side by side, concentrating on speed, power consumption, and overall efficiency to determine whether design truly performs better in real-world applications.

III. SYSTEM GOALS

- **Achieve Reliable Low-Voltage Operation:** To produce SRAM cells that can function reliably at low voltages, lessen the likelihood of read disruptions and write errors.
- **Minimize Power Consumption:** Reduce the amount of leakage power wasted while the system is idle as well as the dynamic power needed while switching.
- **Ensure Fair Technology Comparison:** Build both SRAM cells using the same CMOS technology and settings.

IV. LITERATURE REVIEW

The design of static random access memory (SRAM) has changed a lot so that it can work with ultra-low-power and near-threshold computing applications. Under lower supply voltages, higher leakage, and worse static noise margins (SNM), regular 6T SRAM cells don’t write well. To get around these limits, several modified SRAM bit cell architectures, especially 10T designs, have been suggested to improve stability, leakage performance, and minimum operating voltage (Vmin) [3].

ISBN: 978-81-689089-0-1

Their design employs decoupled read access, differential pre-discharged bit lines, and a highly stacked pull down structure that cuts down on leakage power by a lot. This means that the standby power is only 41 nW at 0.2 V. This research confirms that read decoupling and stacking transistors are effective ways to lower subthreshold leakage. However, the increase in transistor count results in an additional area overhead and layout complexity compared to conventional 6T cells [4].

To address half-select disturb and enhance write-ability in scaled technologies, Lien et al. introduced a cross-point 8T SRAM with adaptive assist techniques [4]. Their design incorporates ripple bit line architecture, binary word line boosting, and adaptive data-aware write-assist mechanisms. The cross-point structure effectively eliminates write half-select disturbance and improves soft-error immunity. Although the design achieves high-speed operation (up to 200 MHz at 0.65 V), it relies heavily on assist circuitry, which increases peripheral complexity, control overhead, and standby power consumption. [1].

In recent years, greater focus has been placed on improving static noise margins and variation tolerance proposed a low-standby-power 10T SRAM cell featuring a cross-coupled Schmitt-trigger and standard inverter combination By separating the read path from the storage nodes and employing pseudo-differential write operation, the design achieves 4.65× improvement in read SNM and 37.35 percent lower leakage power compared to the conventional 6T cell. The enhanced stability under process-voltage-temperature (PVT) variations makes this design suitable for deeply scaled technologies. However, the single-ended architecture increases read delay and introduces area penalty [5].

10-transistor (10T) SRAM bit cell for reliable operation at very low supply voltages. Process variations have a major effect on SRAM performance in modern CMOS technologies, which can increase the minimum operating voltage (Vmin) and reduce reliability. To overcome this problem, the authors developed a variation-tolerant 10T SRAM cell that cans per-form write operations in the subthreshold region without the need for additional help circuits. The proposed architecture temporarily weakens the supply connection during write operations making it easier to modify the stored data at low voltages. It study about several SRAM properties, including read stability, write ability, hold stability, delay and leakage power to assess the design's dependability [6].

V. PROPOSED WORK

A. System Methodology

In order to overcome the well-known drawbacks of the traditional 6T SRAM cell, the proposed work focuses on developing and accessing enhanced SRAM architectures [7]. The literature and problem statement point out that when the 6T cell is operated at low supply voltages, it experiences read disturb problems, deteriorated static noise margin (SNM) and increased leakage. This work conducts a structured comparative implementation of both 6T and 10T SRAM cells under identical technology conditions in order to overcome these limitations shown in Fig 1. This project uses 45 nm CMOS technology in the Cadence Virtuoso environment to design transistor level schematics of the decoupled 10T SRAM and the traditional 6T SRAM. The primary goal is to construct, model, and assess their actual circuit behaviour under the same operating conditions in addition to comparing them theoretically.

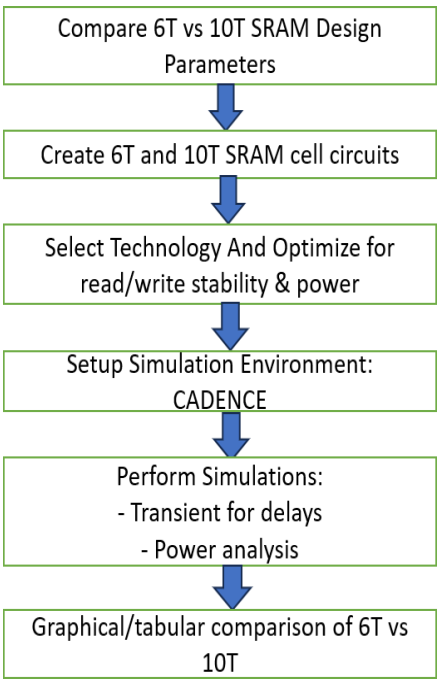

Fig. 1. Block diagram of 6T and 10T SRAM Architecture

B. Hardware Configuration

The SRAM hardware configuration is built using CMOS technology at the transistor level.

6T SRAM: In the conventional 6T SRAM cell, six MOS transistors are arranged as two access transistors and two cross-coupled CMOS inverters.

ISBN: 978-81-689089-0-1

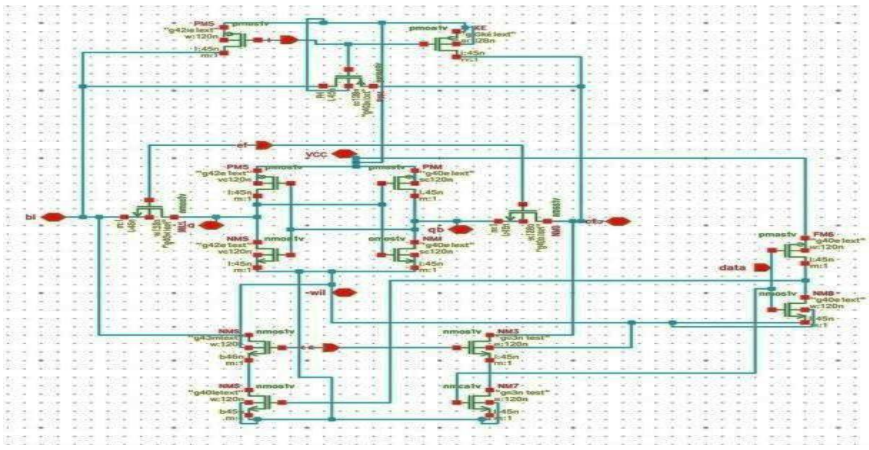

Fig. 2. 6T SRAM Circuit diagram

The cross-coupled inverters produce a bistable latch that can store a single bit of data, while the access transistors connect the internal storage nodes to the complementary bitlines (BL and BLB) that are managed by the word line (WL). Hardware pull-down NMOS and pull up PMOS transistors are sized to allow efficient write operations while maintaining cell stability. By maintaining WL low, hold mode isolates the cell and enables the latch to store data indefinitely. In read mode, WL is asserted and both bitlines are recharged. When the bitlines are in write mode external drivers force them to overwrite the stored value.

10T SRAM: The 10T SRAM cell improves upon the con-ventional design by adding four transistors to divide the read and write functions. The storage element still needs cross-coupled inverters even though the read path is completely isolated from the internal storage nodes

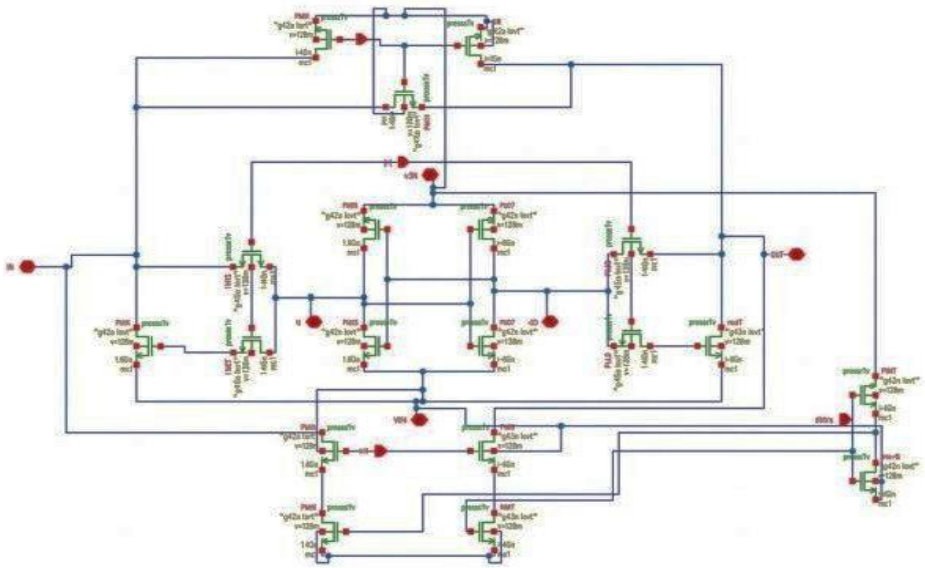

Fig. 3. 10T SRAM Circuit Diagram

The storage element still needs cross-coupled inverters even though the read path is completely isolated from the internal storage nodes.

During read operation, the dedicated read word line activates the read buffer, and the stored data controls the discharge of the read bit line without affecting the latch. During read operation, the dedicated read word line activates the read buffer, and the stored data controls the discharge of the read bitline without affecting the latch.

C. Proposed System Architecture

This 4x4 memory array is constructed from a row by column matrix for 16 identical 10T SRAM cells. This design improves read reliability while maintaining reasonable write performance [1].

During the write operation, a write word line is asserted and data is applied the write bit lines (BL/BLB) to store the new data in the latch. In addition to pre charging a read bits line for the read operation, the read word line is activated. Accurate data sensing is made possible by the read procedure's selective release of the read bit line according to the data that is stored, which does not affect the stored node.

ISBN: 978-81-689089-0-1

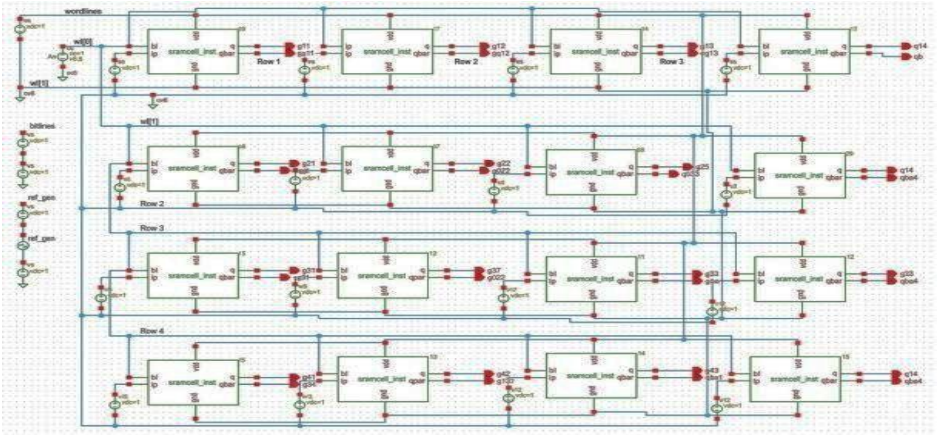

Fig. 4. Proposed Memory array for SRAM

The circuit shows an SRAM memory array with many SRAM cells that are connected by common word lines and bit lines in rows and columns. Some of the inputs are the 16 supply voltage (VDD), the ground reference (VSS).

D. Proposed Memory single cell

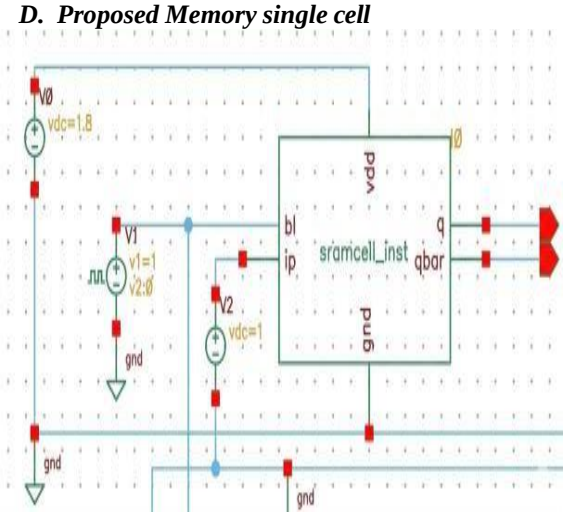

Fig. 5. Proposed Memory single cell

The 6T and 10T SRAM cells use the same ffunctional logic for common memory operations

E. Output Analysis for proposed memory Array

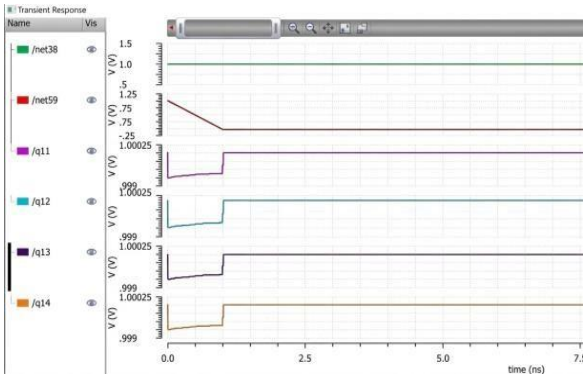

Fig. 6. Transient analysis for 6T SRAM memory cell for input 1

Transient analysis for 6T SRAM memory cell for input 1: The circuit simulates a single SRAM cell test setup to make sure that it can read and write basic data. The memory cell gets its operational power from inputs like the supply voltage (VDD = 1.8 V) and ground. A DC source on the bit line (BL) sends the data value during a write operation.

F. Transient analysis for 6T SRAM memory cell for input 0:

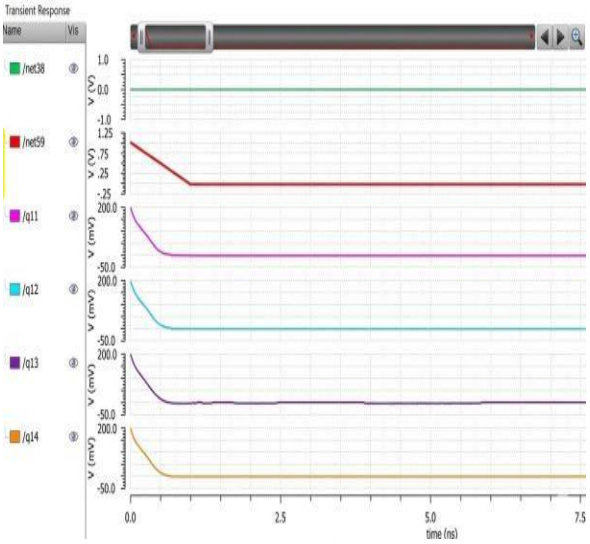

Fig. 7. Transient analysis for 6T SRAM memory cell for input 0

The transient simulation of the 4×4 6T SRAM memory array for logic 0 input was performed over a 7.5 ns window at 1.0 V supply. Net38 is held at logic 0 (0 V), while net59 (write enable) transitions from high to low, triggering the write-to-read operation. During the write phase, all four storage cells are driven to logic 0.

VI. LAYOUT DESIGN

In a Cadence Virtuoso software environment, designs have been CMOS configurations of 6-transistor (6T) and 10-transistor (10 T) SRAM cells.

ISBN: 978-81-689089-0-1

A. 6T SRAM Layout

Both cells utilize cross-coupled CMOS inverters composed of PMOS and NMOS transistors to store a single bit of data.

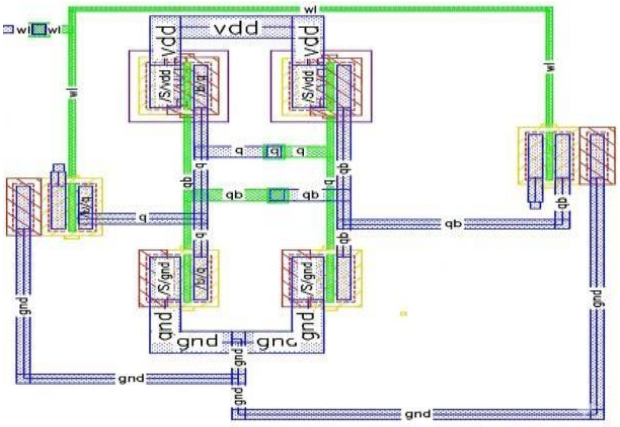

Fig. 8. 6T SRAM LAYOUT

The SRAM cell's outputs are the internal storage nodes Q and QB, which hold complementary logic values. These nodes are made by cross-coupled inverters, which keep data as long as there is power. During a read operation, the value stored at Q and QB is moved to the bit lines. The layout makes sure that latency and stability are as low as possible by keeping these nodes small and well-shielded, lowering leakage, and making them more reliable.

B. 10T SRAM Layout

In contrast, the additional transistors in the 10T SRAM cell split both read as well written paths, improving read Stability and reducing the possibility of reading disturbances over memory access.

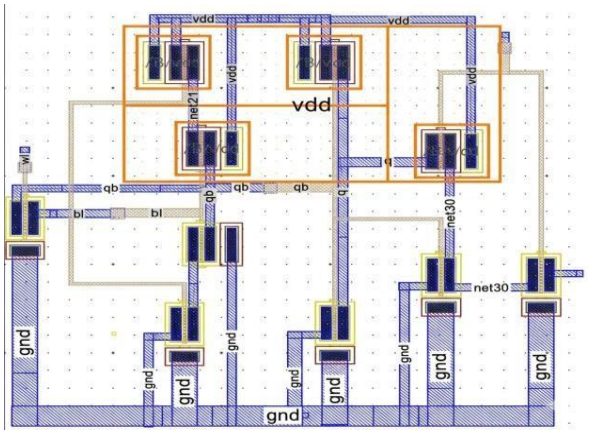

Fig. 9. 10T SRAM LAYOUT

The layouts are organized symmetrically to ensure better matching and reliable operation, thereby facilitating a successful DRC and LVS verification. These arrangement structures can be incorporated into larger SRAM arrays and offer greater stability, performance, as well as memory operation efficiency.

C. RC Extracted

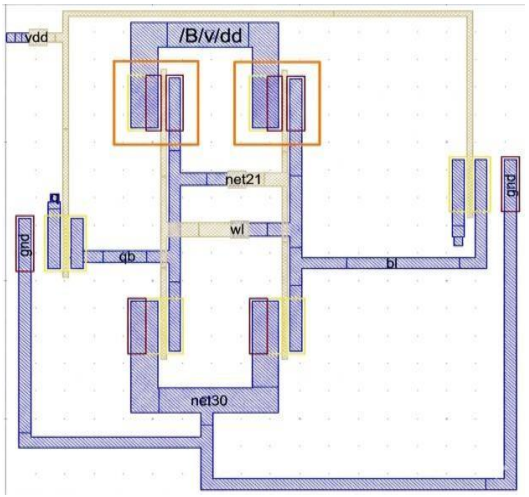

Fig 10(a): RC extracted for 6T SRAM

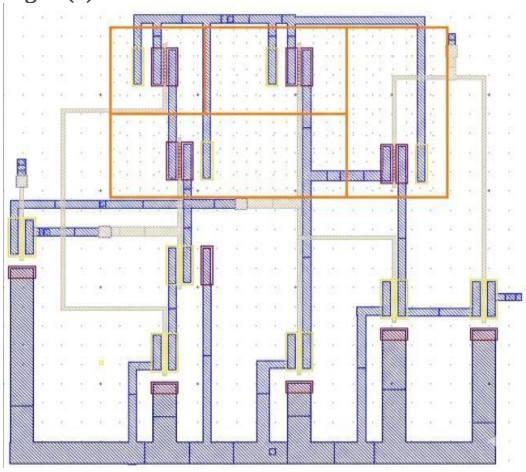

Fig 10(b): RC extracted for 10T SRAM

VII. RESULT AND ANALYSIS

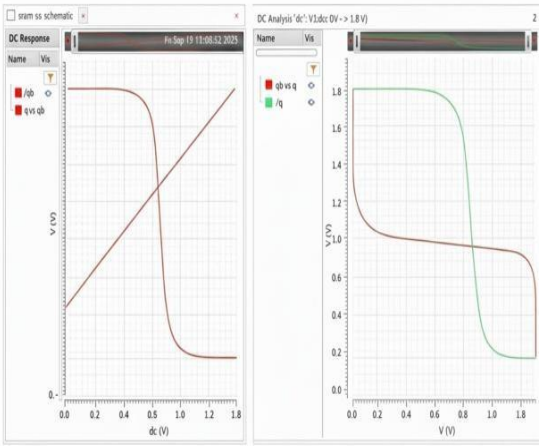

Fig 11(a): DC Analysis of 6T SRAM

The butterfly curve of the 6T SRAM cell was obtained through DC sweep analysis from 0 V to 1.8 V at SS(slow-

ISBN: 978-81-689089-0-1

slow) process corner. The left plot depicts the DC transfer characteristics of QB vs Q and Q vs QB.

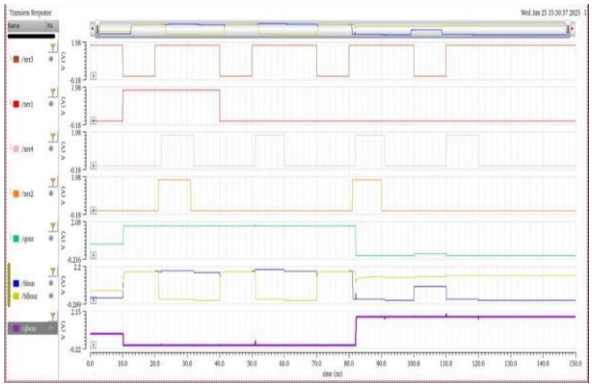

Fig 11(b): DC Analysis of 10T SRAM

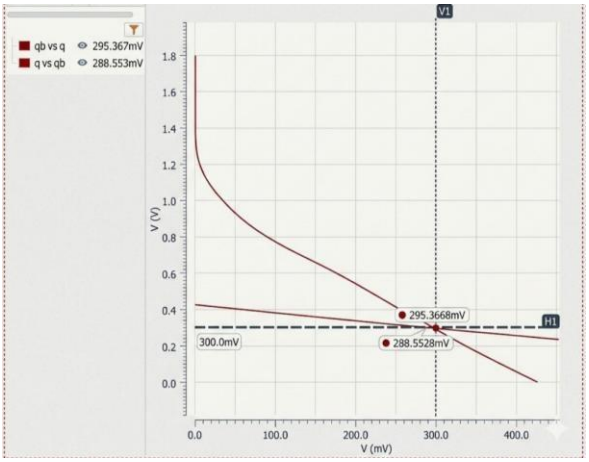

Fig 12(a): Timing Analysis 6T SRAM

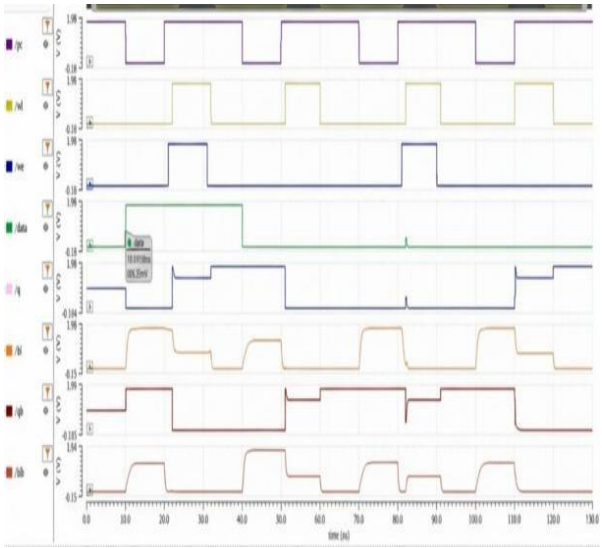

Fig 12(b): Timing Analysis 10T SRAM

The transient simulation of the 10T SRAM cell was performed over a 150 ns window at 1.98 V supply. The signals WL (write word line), read word line (RWL), write enable, precharge, and data serve as control inputs.

TABLE I
PARAMETER ANALYSIS OF 6T AND 10T SRAM CELLS FOR SCHEMATIC (45NM)

Parameter	6T SRAM	10T SRAM
Average(V)	1	1
Dynamic Power(W)	203.4μ	999.9μ
Area (nm^2)	135	225
Delay(s)	732.21p	1.09n

The 6T SRAM cell consumes a power of 631.4 W at a delay of 921 ps, with an area of 135 nm² and an access delay of 732.21 ps [8]. The 10T SRAM cell, on the other hand consumes 999.9 W at 952 ps with an area of 225 nm² and a delay of 1.09ns.

TABLE II
Parameter Analysis of 6T and 10T SRAM Cells for layout(180nm)

Parameter	6T (schematic)	6T (Post Layou t)	10T (Schemati c)	10T (post Layou t)
Area(μm^2)	18	32	30	14
Dynamic Power (μW)	11.5	16	6.5	9
Leakage Power (nW)	120	125	160	165
Read Delay (ns)	0.75	1.02	0.47	0.65
Write Delay (ns)	0.55	0.80	0.80	0.97

The 10T SRAM cell offers improved read stability with a read delay of 0.475 ns and dynamic power of 6.5 μW. Compared to existing works, the proposed design achieves an average power of 11.62 μW. against 898,300 μW, a reduction of over 99.99%, and a write delay of 0.55 ns against 0.67 ns, an improvement of 17.9% [9].

VIII. CONCLUSION

This paper describes the development and implementation of an SRAM memory cell for both 6T and 10T SRAM cells at the schematic and layout levels. Functional verification was carried out using DC and transient analysis to verify steady read and write operations. Key performance information was obtained, including area, power consumption, and propagation delay. Simulation results show that the developed SRAM cell provides reliable performance with suitable trade-offs between power, area, and delay. The provided design flow demonstrates a thorough memory cell creation process that could be extended for SRAM array-level implementation and optimization.

ISBN: 978-81-689089-0-1

Successfully implement the suggested SRAM memory architecture using an array of attached memory cells. We also tested the read and write operations to make sure they functioned correctly.

IX. FUTURE WORK

Future research will focus on utilising supplementary peripheral hardware, including voltage amplifiers and buffer stages, to extend delay analysis from a singular SRAM cell to both row-level and column-level memory operations.

REFERENCES

[1] E. Abbasian and S. Sofimowloodi, "Energy-efficient single-ended read/write 10t near-threshold sram," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 70, no. 5, pp. 2037–2047, 2023.

[2] R. Ranjan and S. L. Maskara, "Design and analysis of 6t sram cell in 45nm and 180nm technologies," International Journal of Research in Electronics and Communication Technology (IJRECT), vol. 9, no. 2, 2020.

[3] Y.-C. Chien and J.-S. Wang, "A 0.2 v 32-kb 10t sram with 41 nw standby power for iot applications," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 8, pp. 2443–2454, August 2018.

[4] N.-C. Lien et al., "A 40 nm 512 kb cross-point 8t pipeline sram with binary word-line boosting control, ripple bit-line and adaptive data-aware write-assist," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 61, no. 12, pp. 3416–3425, December 2014.

[5] E. Abbasian, F. Izadinasab, and M. Gholipour, "A reliable low standby power 10t sram cell with expanded static noise margins," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 69, no. 4, pp. 1606–1616, April 2022.

[6] S. Gupta, K. Gupta, and N. Pandey, "Pentavariate vmin analysis of a subthreshold 10t sram bit cell with variation tolerant write and divided bit-line read," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 10, pp. 3326–3337, October 2018.

[7] S. Gupta, K. Gupta, B. H. Calhoun, and N. Pandey, "Low-power nearthreshold 10t sram bit cells with enhanced data-independent read port leakage for array augmentation in 32-nm cmos," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 3, pp. 978–988, March 2019.

[8] S. Bagali, B. Sravani, B. Kavya, M. B. Varalakshmi, and S. L. A. Reddy, "Design and parametric analysis of 6t sram using 180nm and 45nm technology," in 2023 International Conference on Network, Multimedia and Information Technology (NMITCON). IEEE, September 2023, pp. 1–7.

[9] A. Siddik, S. Pujari, J. Mallidu, P. Chandaragi, A. Huded, and N. Lakkundi, "Performance analysis of cmos sram 6t, 7t and 9t cells using cadence at 180nm technology," in 2024 3rd International Conference for Innovation in Technology (INOCON). IEEE, March 2024, pp. 1–5.

[10] L. Chang et al., "An 8t-sram for variability tolerance and low-voltage operation in high-performance caches," IEEE Journal of Solid-State Circuits, vol. 43, no. 4, pp. 956–963, April 2008.

[11] S. Ahmad, M. K. Gupta, N. Alam, and M. Hasan, "Single-ended schmitttrigger-based robust low-power sram cell," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. 8, pp. 2634–2642, August 2016.

[12] Y. -W. Chiu et al., "40 nm bit-interleaving 12t subthreshold sram with data-aware write-assist," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 61, no. 9, pp. 2578–2585, September 2014.

[13] M.-H. Tu et al., "A single-ended disturb-free 9t subthreshold sram with cross-point data-aware write word-line structure, negative bit-line, and adaptive read operation timing tracing," IEEE Journal of Solid-State Circuits, vol. 47, no. 6, pp. 1469–1482, June 2012.

[14] D. Jeon et al., "A 23-mw face recognition processor with mostly-read 5t memory in 40-nm cmos," IEEE Journal of Solid-State Circuits, vol. 52, no. 6, pp. 1628–1642, June 2017

[15] Y. Han et al., "Radiation hardened 12t sram with crossbar-based peripheral circuit in 28nm cmos technology," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 7, pp. 2962–2975, July 2021.

[16] T.-H. Kim, J. Liu, J. Keane, and C. H. Kim, "A 0.2 v, 480 kb subthreshold sram with 1 k cells per bitline for ultra-low-voltage computing," IEEE Journal of Solid-State Circuits, vol. 43, no. 2, pp. 518–529, February 2008.

[17] G. Pasandi and M. Pedram, "Internal write-back and read-before-write schemes to eliminate the disturbance to the half-selected

ISBN: 978-81-689089-0-1

cells in srams," IET Circuits, Devices & Systems, vol. 12, no. 4, pp. 460–466, July 2018.

[18] M. Karamimanesh, E. Abiri, K. Hassanli, M. R. Salehi, and A. Darabi, "A write bit-line free sub-threshold sram cell with fully half-select free feature and high reliability for ultra-low power applications," AEU - International Journal of Electronics and Communications, vol. 145, p. 154075, February 2022.

[19] J. P. Kulkarni, K. Kim, and K. Roy, "A 160 mv robust schmitt trigger based subthreshold sram," IEEE Journal of Solid-State Circuits, vol. 42, no. 10, pp. 2303–2313, October 2007

Cite this article as:

Mandala, Konka *and et.al. "Analytical Comparision of Design Parameters in 6T and 10T SRAM Architectures and Memory Array", Proceedings of 13th international conference on Microelectronics, Circuits and Systems, Micro2026 (Vol-II)*

Displayed as online on 21st August 2026.

Link: http://actsoft.org/science/micro2026-pro/362-micro2026.pdf

@Copyright to 'Applied Computer Technology', Kolkata, WB, India. Website: https://actsoft.org, Email: info@actsoft.org

ISBN: 978-81-689089-0-1