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Assessment of Low Voltage Performance Metrics in Multiple 8T SRAM Architectures

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ABSTRACT

Various 8T SRAM cell designs are comparatively analyzed to determine the most performance-efficient configuration. Monte Carlo simulations were performed at the 22-nm technology node to evaluate key design metrics. The Read Stack 8T (RS8T) and Low Power 8T (LP8T) cells demonstrate the shortest read access time (TRA), whereas the Zigzag 8T (ZZ8T) exhibits the longest. The Differential Data-Aware Power-Supplied 8T (D2AP8T) achieves the fastest write access time (TWA), while the Feedback Control 8T (FCS8T) shows the slowest. Among all designs, D2AP8T also has the lowest hold and write power consumption, making it the most efficient 8T SRAM cell overall, with superior write performance and energy efficiency at the cost of slightly higher read access time.

Keywords: Hold Power; Read Access Time; Write Access Time; RSNM; WSNM; Write Power.

I. INTRODUCTION

Advancements in technology have enabled the development of microprocessors with significantly enhanced performance. In order to keep up with their performance, high functioning memory needs to be developed. To meet this gap between memory and microprocessor, SRAM cells are fabricated on the same die as the microprocessor. They serve as the cache memory and are faster than DRAM. As per International Technology Roadmap for Semiconductors (ITRS) [1], SRAM cell occupies 90% of the chip area. With such a huge portion being occupied, they account for majority of the power consumption. With the growth of portable device technology like mobile phones the need for low power consuming circuits has increased. In SRAM cells more than 40% of the total power consumed is wasted as leakage power [2]-[4]. Hence, a low power consuming, high speed, read/write stable memory meeting the area constraints is desirable. Some of the design parameters of SRAM are conflicting in nature.

In a 6T SRAM cell there is a conflict between read and write stability. For read stability the pull-down MOSFETs need to be stronger than the pass transistors else read failure occurs [5]. And for write stability the pass transistors need to be stronger than the pull-up MOSFETs. Since the pass transistors used for read and write operation are same in 6T cell the above criteria is not fulfilled simultaneously. In order to mitigate this problem a lot of SRAM cells with higher number of transistors like 8T, 9T, 10T etc. have been proposed in the literature. In few 8Ts two extra transistors are used in order to provide a separate disturb free path for reading, in few others, two transistors are used for differential power supply. A large number of 8T SRAM cells have been proposed. In this work we investigate different parameters of various already proposed 8T SRAM cells and try to come to the conclusion that which one is the best. The parameters which are compared are read access time (TRA), write access time (TWA), write power (WPWR), hold power (HPWR), read static noise margin (RSNM) and write static noise margin (WSNM). These comparisons are made in 22-nm technology and the simulations have been done in SPICE (5000 Monte Carlo simulations) using the 22-nm PTM (Predictive Technology Mode) [6].

The remainder of this paper is organized as follows. Section II describes the cell topologies of five 8T SRAM designs. Section III presents the simulation results and provides a parameter-wise comparison of these cells. Section IV offers a comparative analysis of the electrical quality metrics (EQM) for the various 8T SRAM cells [7]. Finally, Section V summarizes the conclusions drawn from the study.

II. CELL TOPOLOGIES

This section briefly describes the topologies of the five 8T SRAM architectures considered in this study.

A. Read stack 8T (RS8T) SRAM Bitcell:

Fig. 1 refers to the RS8T SRAM cell [8], which has a two-transistor read stack (MN5/6) additional to the conventional 6T cell. The original 6T word line is used exclusively for a write operation while a separate read line is used for single ended read operation. Read disturb, a major problem of 6T is effectively eliminated with this configuration. Flipping of cell contents during read operation doesn't occur in this 8T cell. As a result, static noise margin is improved. It has an exceptional variability tolerance. Due to ideal read stability and enhanced

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write ability of this 8T SRAM cell a good yield can be achieved at low operating voltages. This eliminates the need for secondary or dynamic power supply.

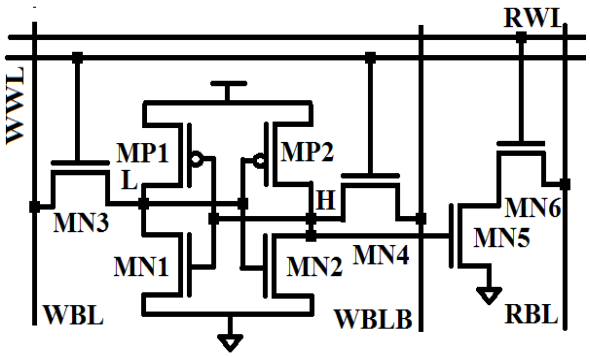

Fig. 1. Circuit diagram of single ended read stack 8T-SRAM cell (RS8T) for low-voltage operation.

Before a read operation, read bit line RBL is pre-charged initially to V_{DD} (say, storage node L is storing '0' and H is storing '1' prior to read operation). When RWL becomes high MN6 is on (due to RWL=1) and MN5 is on (due to H=1). Now RBL discharges slowly to zero through the transistors MN6 and MN5 which is sensed by a sense amplifier. Write operation of RS8T cell is similar to that of 6T's write operation. Consider node L stores logic '0' and node H stores '1' prior to write operation. Then for writing '1' on node L, BL is driven high while BLB is pulled down to ground by write driver. When WWL becomes high, MN3 is on and BL finds a path to discharge through MN3 and MN1. As a result, voltage rises at node L and once node L reaches 1, inverter MP2-MN2 is on and H flips to '0'.

B. Differential data aware power supplied (D2AP) 8T SRAM Bitcell:

The differential data aware power supplied D2AP 8T cell [9] is shown in Fig. 2. This cell has two additional PMOS transistors MP3 and MP4 through which the cross coupled inverters are powered by the bit line pair instead of sharing the same power line. MP3 and MP4 act as two PMOS switches between the pull up transistors and bit line pair. A second word line ZWL is used for gating MP3 and MP4. With this circuit V_{DDmin} is considerably lowered. D2AP cell has a hold static noise margin (HSNM) similar to that of the conventional 6T cell.

Both BL and BLB are pre-charged to V_{DD} prior to read operation (say, prior to read operation node L is storing '0' and node H is storing '1'). During a read operation ZWL is made low so that MP3/4 are ON. When WL becomes high, BL discharges through MN3 and MN1 while BLB is kept high. Here MP1 gets its source voltage from BL through MP1. The read operation is differential and as a result better noise immunity and faster read access time can be observed.

For a write '0' operation where '0' is written on node L (assuming that '1' is stored on node L and node H stores '0' prior to write operation), BL is pulled down to ground while BLB is kept high. Both MP3 and MP4 are ON during write operation. BL being held at 0V, source voltage of MP1 is reduced turning it weak to maintain node 'L' at 1 and trip point of inverter L is lowered increasing its write margin. MP2 source voltage is maintained at V_{DD} to enhance the pull-up speed for node 'H'.

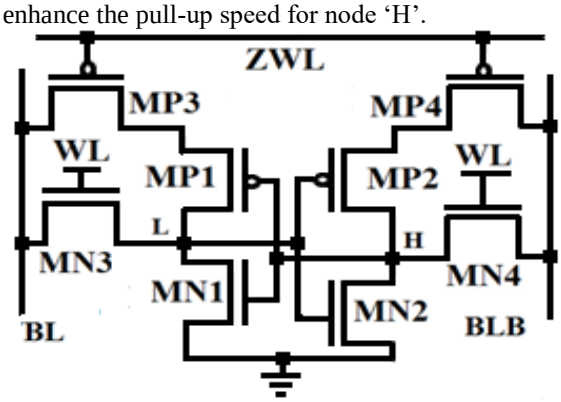

Fig. 2. D2AP 8T SRAM cell is powered by bit-line pair which applies differential data aware supply voltage to the cross-coupled inverters which increases write margin stability

C. Low power 8T (LP8T) SRAM Bitcell:

Fig. 3 refers to the LP8T which is similar to conventional 6T [10] with two extra buffer transistors (MN6/5), a tail transistor (MN7) and a WWLB line. This buffer transistors improve read stability as it provides an extra pull-down path to discharge. And tail transistor improves hold power due to stack effect. For the read operation pre-charging of BL and BLB is done, WWL is raised to V_{DD} and WWLB is lowered to ground. Pertaining to the node storing high MN5/6 is on. BLB/BL discharges through access transistors MN3/4 with two paths, one through MN5/6 and the other through MN1/2.

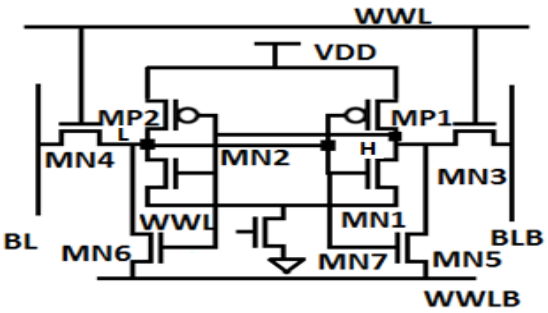

Fig. 3. Low power dissipated 8T SRAM cell (LP8T) where stacking effect reduces the power dissipation.

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Because of the two paths available a faster read operation is possible. For the write operation where '0' is written on node L (it is assumed that node L stores '1' and node H stores '0' prior to write operation), WWL is raised to V_{DD}, WWLB is kept low by the write driver. H node discharges through MN4 and BL and voltage at node L rises towards V_{DD} through MN3.

D. Zigzag 8T SRAM (ZZ8T) cell:

The ZZ8T SRAM cell [11] comprises of a 6T cell and a 2T decoupled read-port transistors as shown in Fig. 4. These 2 transistors transfer data stored at the L and H nodes to RBLB and RBL nodes.

For the read operation RWL is given a low pulse and RBL and RBLB are pre-charged initially. Considering node L stores '1' and H stores '0' prior to read operation then MN5 is on while MN6 is off. As a result, RBLB is pulled down while RBL remains at V_{DD}. Now considering node L stores '0' and node H stores '1' prior to read operation then MN6 is on and hence RBL is discharged and RBLB remains high resulting in a successful read operation.

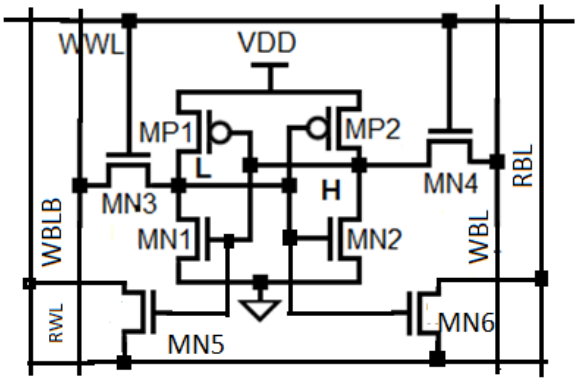

Fig. 4. Zigzag 8T SRAM cell (ZZ8T) with decoupled differential sensing and fast writing scheme.

For the write operation, WWL is kept high and hence the pass transistors are on. The write operation is similar to that of a conventional 6T SRAM.

E. FCS8T SRAM Bit-cell

The FCS8T SRAM cell [12] as shown in Fig. 5 has two cross coupled inverters each comprising three cascaded transistors. The true storing node is decoupled from the bit line which suspends read disturb. Single ended write with dynamic feedback cutting and read decoupling are the key features of this cell. Read and write paths are different. Write ability is enhanced and read disturb is eliminated with this SRAM cell. Separate read and write lines RWL and WWL, two additional lines FCS1 and FCS2 to control feedback cutting transistors are used in this cell.

During a read operation where '1' is stored on node Q and '0' is stored on node QB initially, RBL is pre-charged to V_{DD}. Both the lines FCS1 and FCS2 are held at ground. RWL when made high turns ON the M3 transistor and M4 is also turned ON due to Q=1. So RBL will discharge through M3 and M4 which will be sensed by an inverter sense amplifier.

For writing '1' on node Q which is assumed to store '0' prior to write operation, WBL is pulled up high.

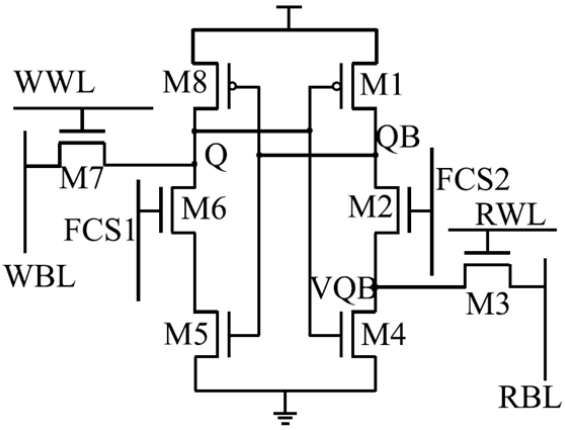

Fig. 5. Single ended 8T SRAM cell (FCS8T) with dynamic feedback control scheme which enhances the static noise margin.

When WWL is raised high, current flows from WBL to Q resulting in a voltage rise at Q. The line FCS1 is pulled down and FCS2 is made high due to which M2 conducts connecting QB to the ground.

III. SIMULATION RESULTS AND DISCUSSION

In this section, the simulation results of the five 8T SRAM cells are presented. The parameters considered for comparison include read access time (TRA), write access time (TWA), write power (WPWR), hold power (HPWR), read static noise margin (RSNM), and write static noise margin (WSNM).

A. Simulation Setup:

International Technology Roadmap for Semiconductors (ITRS) [1] is an organization that is responsible for setting the blue print of the semiconductors industry. It suggests certain variations in channel width (W), supply voltage (V_{DD}), oxide thickness (t_{OX}), threshold voltage (V_t), channel length, (L) and dopant concentration (*NDEP*). A total of 5000 Monte Carlo (MC) simulations are performed by incorporating variations in the previously mentioned parameters, with distinct model files generated for each parameter set using the Predictive Technology Model (PTM). [6]. Monte Carlo simulation enables the analysis of both global and local variations in device parameters. Using *.MEASURE* statements, circuit designers can statistically evaluate key performance metrics such as

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propagation delay, power dissipation, power–delay product, and energy–delay product by extracting parameters including mean, median, variance, standard deviation, average deviation, as well as minimum and maximum values. All simulation results reported in this work are obtained using models corresponding to the 22-nm technology node. All design metrics are computed at a supply voltage of 0.8 V while accounting for 10% supply voltage fluctuations. The methodology is based on the technology scaling and device parameter projections provided by the 2011 edition of the International Technology Roadmap for Semiconductors (ITRS). Therefore, the operating supply voltage in the simulations spans the range from 0.72 V to 0.88 V.

B. Analysis of Read Access Time (TRA):

Read Access Time is the measure of the time interval when voltage difference between RBL and voltage supply (V_{DD}) becomes greater than or equal to 50 mV when RWL starts increasing. A differential sense amplifier with one input at supply voltage and the other at RBL is used to detect the difference of 50 mV [13].
A comparative analysis of the read access time (TRA) for different 8T SRAM cell configurations is presented in Table I, with the corresponding simulation results illustrated in Fig. 6. Examination of both the tabulated values and graphical trends indicates that the RS8T and LP8T cells exhibit the minimum TRA, thereby offering the fastest read performance among the evaluated architectures.

TABLE I.
READ ACCESS TIME (TRA)

V_{DD}	RS8T (ns)	D2AP8T (ns)	ZZ8T (ns)	LP8T (ns)	FCS8T (ns)
0.72V	0.35	0.36	0.51	0.34	0.36
0.76V	0.33	0.35	0.47	0.32	0.35
0.80V	0.29	0.33	0.44	0.29	0.33
0.84V	0.24	0.31	0.41	0.25	0.32
0.88V	0.20	0.27	0.39	0.22	0.28

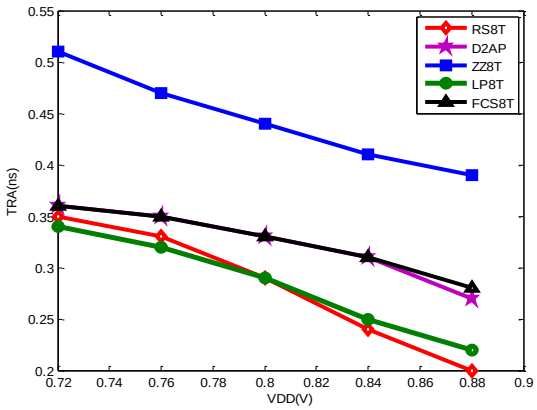

Fig. 6. Analysis of read access time versus supply voltage (V_{DD}).

C. Analysis of Write Access Time (TWA):

The write speed of 8T SRAM cells is evaluated by comparing their write access time (TWA), which indicates the effectiveness of the write path, the drive capability of the access transistors, and the capability of the bit-lines to reliably modify the stored data under reduced supply voltage and process variations [14]. The write access time (TWA) results obtained at different supply voltage levels are presented in Table II, while the corresponding simulation outcomes are depicted graphically in Fig. 7. An analysis of both the tabulated data and graphical trends indicates that the D2AP8T cell achieves the minimum TWA across the evaluated voltage range, thereby demonstrating superior write speed compared to the other 8T SRAM cells.

TABLE II.
WRITE ACCESS TIME (TWA)

V_{DD}	RS8T (ns)	D2AP8T (ns)	ZZ8T (ns)	LP8T (ns)	FCS8T (ns)
0.72V	0.69	0.55	0.72	0.72	1.07
0.76V	0.67	0.5	0.7	0.7	0.99
0.80V	0.66	0.47	0.69	0.68	0.94
0.84V	0.67	0.44	0.68	0.67	0.9
0.88V	0.68	0.41	0.689	0.66	0.86

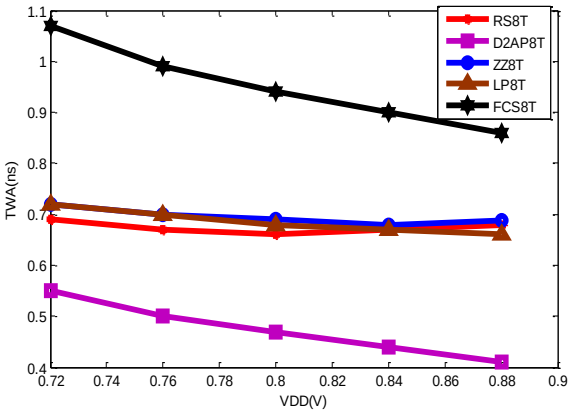

Fig. 7. Analysis of write access time (TWA) versus supply voltage (V_{DD}).:

D. Write power analysis

Power loss during read and write operations in SRAM cells are predominantly dynamic in nature and constitute the major portion of the total power dissipation. During the read operation, the bit-lines (BL/BLB) experience only a small voltage swing, typically around 50 mV, which helps limit dynamic power consumption. In contrast, the write operation involves full charging and discharging of the highly capacitive bit-lines, leading to significantly higher switching activity and energy dissipation. As a result, the write operation accounts for the dominant share of dynamic power loss, with nearly 60% of the

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total dynamic power being consumed during write cycles due to repeated bit-line transitions and stronger drive requirements [15].

The capacitance of the bit lines C_{BL} and C_{BLB} is due to $C_{D/S}$ (drain/source capacitance), C_{int} (interconnect capacitance) and C_{con} (contact capacitance).

The equation for CBL is given as

$$C_{BL} = C_{BLB} = C_{D/S} + C_{\text{int}} + C_{con}. \quad (1)$$

Dynamic power during write operation to any bit line is given as

$$P_{WRITE} = \alpha_{WRITE} \times C_{BLB} \times V_{DD}^2 \times F_{WRITE} \quad (2)$$

Where α_{WRITE} is the switching factor and F_{WRITE} is the frequency of writing.

A comparative evaluation of write power consumption is carried out for different 8T SRAM cell architectures, with the corresponding results summarized in Table III and illustrated graphically in Fig. 8 to enhance clarity of comparison. The data reveal that the D2AP8T cell exhibits the minimum write power consumption among the evaluated designs.

TABLE III.
WRITE POWER ANALYSIS (WPWR)

V_{DD}	RS8T (uW)	D2AP8T (uW)	ZZ8T (uW)	LP8T (uW)	FCS8T (uW)
0.72V	1.1	0.03	1.15	1.1	0.09
0.76V	1.4	0.034	1.51	1.5	0.131
0.80V	1.9	0.038	1.96	1.9	0.19
0.84V	2.4	0.041	2.51	2.4	0.27
0.88V	3.1	0.045	3.17	3	0.375

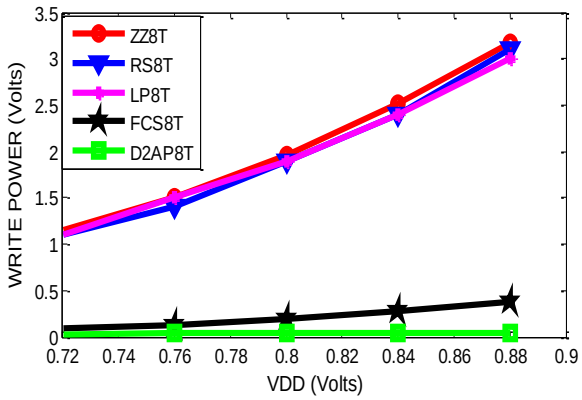

Fig. 8. Write power analysis versus supply voltage (V_{DD}).

E. Hold power analysis (HPWR)

In SRAM arrays, most memory cells spend a large fraction of time in the hold state, during which they remain inactive. As a result, power dissipation during the hold mode constitutes a significant portion of the total memory power consumption. This power loss is mainly due to leakage currents in the transistors responsible for maintaining the stored data, and it becomes increasingly significant in deeply scaled technologies and under low supply voltage conditions. Therefore, reducing hold power is essential for the design of energy-efficient SRAMs, particularly for low-power and always-on system applications [15].

A comparative evaluation of hold power consumption across various 8T SRAM cell architectures is conducted, with the resulting data summarized in Table IV and illustrated graphically in Fig. 9. Analysis of both the tabulated results and graphical trends indicates that the D2AP 8T cell exhibits the lowest hold power consumption among the considered designs.

TABLE IV.
HOLD POWER (HPWR)

V_{DD}	RS8T (nW)	D2AP8T (nW)	ZZ8T (nW)	LP8T (nW)	FCS8T (nW)
0.72V	2.5	0.0012	2.45	0.25	0.88
0.76V	3.5	0.0014	3.47	0.29	1.27
0.80V	4.9	0.0015	4.94	0.34	1.85
0.84V	7.1	0.0017	7.02	0.39	2.73
0.88V	10	0.0018	10.19	0.46	4.07

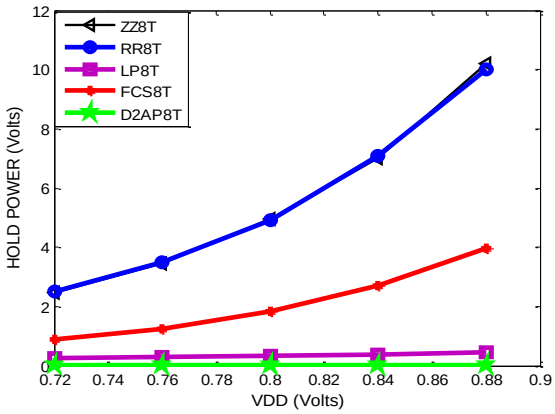

Fig. 9. Hold power analysis versus supply voltage (V_{DD}).

F. Characteristics of the SRAM Architecture

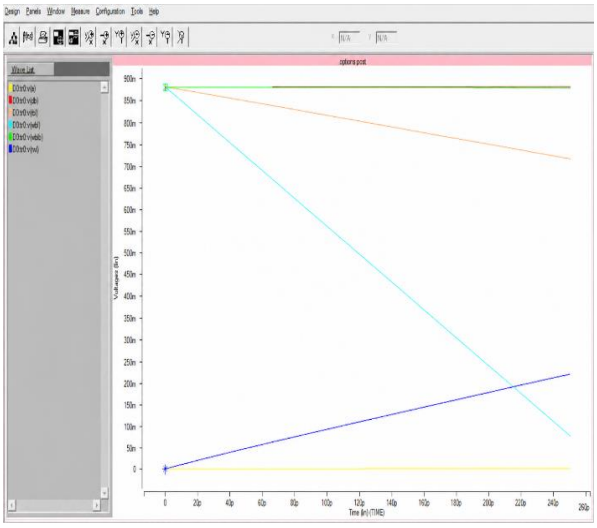

Fig. 10. Simulated Snapshot of Read Operation

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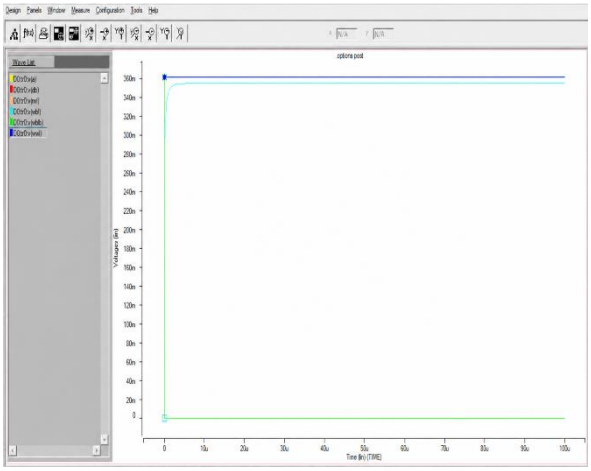

Fig. 11. *Simulated Snapshot of Write Operation*

Fig. 10 and 11 shows that the simulated snapshots of the Read and write Operation with one among the SRAM cell in 22nm technology.

IV. NUMERICAL COMPARISONS AGAINST BASELINE ARCHITECTURES

Table IV.
COMPARISON AGAINST BASELINE ARCHITECTURES

Metric	D2AP8T	Best baseline	Improvement
Write Access Time	0.47 ns	RS8T = 0.66 ns	28.8% lower
Write Power	0.038 µW	FCS8T = 0.19 µW	80.0% lower
Hold Power	0.0015 nW	LP8T = 0.34 nW	99.6% lower
Read Access Time	0.33 ns	RS8T = 0.29 ns	13.8% slower

At the nominal supply voltage of 0.8 V, the D2AP8T SRAM cell achieves a write access time of 0.47 ns, representing a 28.8% reduction compared to the RS8T cell (0.66 ns), 31.9% reduction compared to LP8T (0.69 ns), and 50.0% reduction compared to FCS8T (0.94 ns). Furthermore, the write power is reduced by approximately 80% compared to FCS8T and about 98% compared to RS8T and LP8T. The hold power is also significantly lower, providing approximately 99.6% reduction compared to LP8T and over 99.9% reduction compared to RS8T and ZZ8T. However, the read access time is about 13.8% higher than RS8T and LP8T, indicating a trade-off between energy efficiency and read speed.

V. CONCLUSION

A comprehensive comparison of key performance metrics, including read access time (TRA), write access time (TWA), hold power, and write power, is carried out for five different 8T SRAM cell architectures, namely ZZ8T, D2AP8T, FCS8T, LP8T, and RS8T. Based on application-specific requirements, SRAM cells exhibiting lower access delays and reduced power consumption are preferred. The analysis of the simulation results indicates that the D2AP8T SRAM cell is the most suitable choice for low-power operation among the evaluated designs. It demonstrates significant improvements in write access time, hold power, and write power compared to the other 8T SRAM cells. However, these benefits are achieved at the expense of a comparatively higher read access time. This trade-off highlights the suitability of the D2AP8T cell for energy-constrained applications where power efficiency is prioritized over read speed. Future work will focus on extending the proposed D2AP8T SRAM architecture to advanced technology nodes and evaluating its performance under process, voltage, and temperature (PVT) variations. In addition, the integration of the proposed cell into larger SRAM arrays and the investigation of its suitability for ultra-low-power and near-threshold computing applications will be explored to further validate its practicality.

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