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Design of Energy Efficient D-Latches for Low Power Applications

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ABSTRACT
Energy-efficient D latch design is crucial for low-power VLSI applications, as latches form the core of sequential circuits and memory elements. This paper presents the design and comparative analysis of 7T, 6T, and 5T D latches optimized for low-power operation. The designs are implemented and simulated using Cadence Virtuoso in 45 nm CMOS technology with a supply voltage of 1V. The performance is analyzed based on power dissipation, propagation delay, and Power delay product. Compared to the 6T D-latch, it is observed in 7T D-Latch that there is -99.9978% reduction in power dissipation and increase in delay by 17.704%. Similarly, when compared to the 6T D-latch, it is observed in 5T D-latch that there is -99.9973% reduction in power dissipation and increase in delay by 16.704%. Also, a 4-bit Serial-In Serial-Out (SISO) shift register is implemented using the D latch designs. The shift register performance is analyzed in terms of power, delay, and PDP. Results indicate that the 5T latch-based shift register achieves the minimum PDP of 95.3×10^{-19}, making it highly suitable for low-power VLSI applications.

Keywords*—VLSI, Low-Power Design, Energy-Efficient Circuits, D Latch, Shift Register, Cadence Virtuoso, Power–Delay Product*

I. INTRODUCTION

Low-power and high-speed sequential and memory elements are essential components of the modern VLSI systems that aim for energy-efficient digital applications. The D latch is a fundamental element widely used in the sequential circuit elements for data storage, timing control, and synchronization. Reducing power consumption without compromising performance has become a crucial challenge as CMOS technology continues to scale. Power Delay Product (PDP) is an effective measure that comprehends the trade-off between power consumption and propagation delay.

This paper, 5-transistor (5T), 6-transistor (6T), and 7-transistor (7T) D latch architectures are designed and analyzed using Cadence Virtuoso in 45 nm CMOS technology. To determine the best energy-efficient latch design, important performance metrics such as power consumption, propagation delay, and PDP are evaluated. To study the impact of latch architecture at the system level, a 4-bit Serial-In Serial-Out (SISO) shift register is designed separately in Cadence Virtuoso Software using 5T, 6T, and 7T D latches. The power consumption, delay, and Power Delay Product (PDP) of each SISO shift register are evaluated, and the results have been compared. SISO is commonly used in serial data communication, data buffering, timing synchronization, and peripheral interfacing. In such serial systems, PDP is a critical parameter, as frequent clocking and multi-stage data propagation directly affect the energy consumed per bit transfer. Simulation results have been obtained from Cadence Virtuoso provide a comprehensive comparison of the proposed D latch architectures and SISO shift registers in terms of power consumption, delay, and PDP, demonstrating their suitability for low-power VLSI system design.

II. LITERATURE REVIEW

Previous studies on the architectures of D-latches have targeted the reduction of power dissipation, propagation delay, and silicon area by minimizing transistors. In standard 7T latches, stability and performance improve at the cost of power consumption, while in 6T and 5T architectures, power dissipation and PDP improve. [1]. The previously proposed techniques of D-latch and shift-register architectures aimed at reducing power and delay by optimizing the latch structure. Feedforward and latch-based designs improve energy

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efficiency by reducing switching activity and critical path delay. These studies have motivated compact D-latch implementations for low-power SISO shift registers [2]. The paper proposes optimized designs for D latch and shift registers in order to improve the design in terms of area, delay, and energy consumption through the optimal cost function method. Recent studies proved that minimizing the complexity and delay for sequential circuit design can improve its efficiency significantly[3]. The use of N-parallel NMOS discharge paths in the design of D-latches results in superior performance improvement due to large discharge current. In prior research, it has been observed that such a design increases area and power overhead because of multiple transistors in parallelAs such, prior research stresses the need for efficacy in designing latches without incurring large performance overheads in area and power [4]. The pulsed latch-based shift registers shows that while pulsed latches have area and power efficiency over latch-based designs, the sensitivity of pulsed latches to variations in the width of the clock pulse is high. This is because small variations in pulse widths can cause setup and hold time errors in pulsed latch circuits when used for high-speed processing [5]. The paper reviews earlier D-latch and shift register designs that use MCML and folded latch architectures to achieve high-speed and reliable operation. However, existing approaches often involve higher power consumption and complexity, motivating the need for compact and energy-efficient D-latch–based shift register designs in scaled CMOS technologies [6]. The paper analyzes flip-flop and latch-based shift register designs, concluding that latches offer advantages in terms of area and power efficiency. However, it is limited to structural analysis and overlooks critical VLSI design factors like process, voltage, and temperature variability, emphasizing the need for a comprehensive study on low-power shift register implementations using D-latch [7]. The paper will present different low-power and area-efficient architectures for shift registers with emphasis on the use of pulsed D latches rather than flip-flops to reduce power and design complexity. Existing literature has proven that latch-based design reduces power dissipation and delay with minimal clock and transistor switching activities. This will be beneficial for designing energy-aware D latch-based shift registers for implementation in low-power VLSI systems [8]. This paper focuses on design approaches using reversible logic in order to reduce delay and hardware complexity in shift registers. Various studies have shown that using reversible logic in designing D flip-flop-based shift registers minimizes delay by reducing switching activity[9]. This paper particularly addresses the design of shift registers based on reversible logic to maintain less delay and hardware. Indeed, the importance of optimizing latch and flip-flop configurations in achieving energy-efficient shift register-based VLSI design cannot be undermined [10].

III. STANDARD 6T D LATCH SCHEMATIC

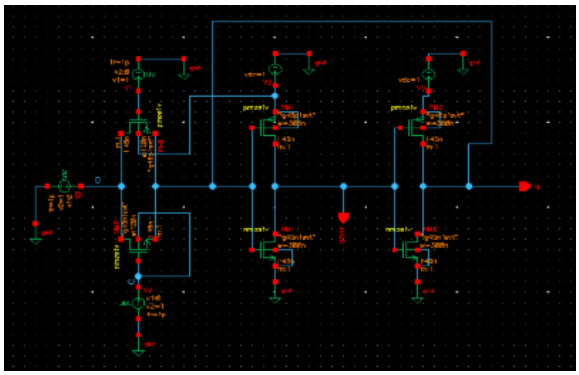

Figure 1. Schematic of 6T D Latch Design

The standard 6T D latch design Figure 1 consists of one clock-controlled input path and one inverter combination for feedback, acting as a storage device. Thus, an inverter pair, with complementary PMOS–NMOS transistors, acts like a bistable storage device that can store the logic value. The control input to this latch is provided through the clock signal C and input data D. Thus, at the high state of the clock signal, an active state exists in the latch and the input data propagates directly to the output. However, when the clock signal changes its state to low, the input path is disabled and the feedback inverter pair forms a closed loop. This is the hold state wherein the inverter combination continuously self-feeds the previously stored value by means of the reinforcing action of the inverter stage. During this hold state, the PMOS transistors provide the required voltage supply to the node in order to retain a stored logic ‘1’, whereas the NMOS transistor does this job in order to retain a stored logic ‘0’. The reinforcing action enables full voltage swing and provides stable data retention with an increased noise immunity. However, the presence of the additional inverter pair slightly increases transistor count and area, leading to marginally higher power

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consumption compared to simpler latch structures.

IV. 7T D LATCH SCHEMATIC

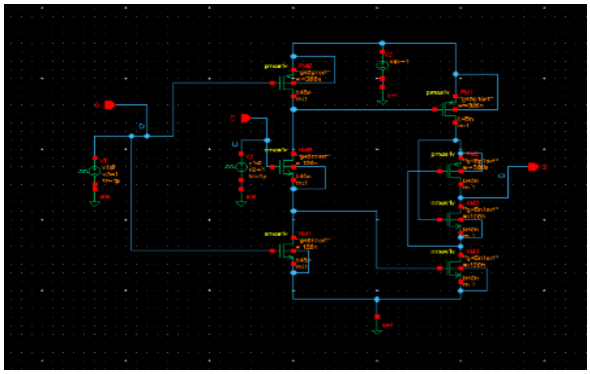

Figure 2. Schematic of 7T D Latch Design

The schematic of the 7T D latch Figure 2 is designed in such a way that it consumes less power and more reliable data storage while at the same time it uses a very small number of transistors. The circuit comprises of seven MOS transistors - 4 NMOS transistors and 3 PMOS transistors and the arrangement of these seven transistors forms the basis where the data input/output is controlled by a single clock signal C, as shown in Fig. 2. As per the circuit functioning when the clock signal C gets activated (high), the latch works in the mode of transparency and thus allows the data at the input D to be transferred to the output Q node. During this operation, the NMOS transistor controlled by the clock makes the input and the internal stored node conductive. With an input at logic '0', the NMOS path to ground gets activated, thus discharging the internal node leading to an output of logic '0', while the PMOS devices are left OFF. Conversely when the input is at logic '1' the PMOS pull-up transistor gets activated, thus drawing the charge of the storage node up to V_{dd} and consequently the output being at logic '1'. When the clock signal C is set low, the latch enters its hold mode, thus cutting off the input from the output. The traditional latch design requires additional leakage-controlled transistors or complementary output stages to provide stable output, on the contrary, the proposed 7T D latch provides a stable single-ended output directly. The efficient arrangement of transistors which is characterized by a non-switched state resulting in low power loss dynamically and statically thus leading to improved reliability of the latch.

V. OPERATION OF 5T D LATCH SCHEMATIC

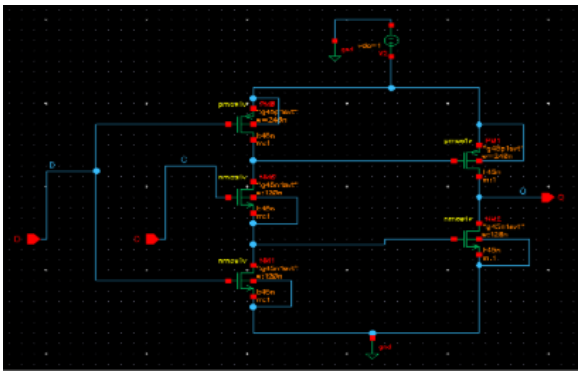

Figure 3. Schematic of 5T D Latch Design

The 5T D Latch design Figure has less area compared with the other two D Latches making it suitable for the SISO application. The working of the 5T D latch is controlled by the clock signal C and input data D. When the clock signal is high, the latch is in an active state, which allows the input data to get passed to the output. For an input of logic '0', transistors PM0, NM0, and NM2 turn ON, pulling the output logic to be '0', while NM1 and PM1 remain OFF. When the input is logic '1', transistors NM0, NM1, and PM1 turn ON, establishing the charging path that drives the output to be logic '1'. When the clock is low, the latch will be in the hold state. The output value is retained as the previously stored state because only PM0 and NM1 stay ON for inputs "0" and "1," respectively, while the other transistors are OFF. This function contributes to the 5T D latch's decreased power consumption by ensuring accurate data storage with less switching activity. Thus, it makes the 5T D Latch suitable for the low-power applications.

VI. SERIAL IN SERIAL OUT SHIFT REGISTER

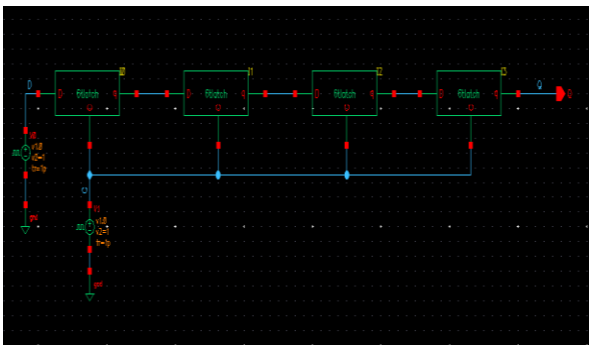

Figure 4. 6T D Latch–Based Serial-In Serial-Out Shift Register

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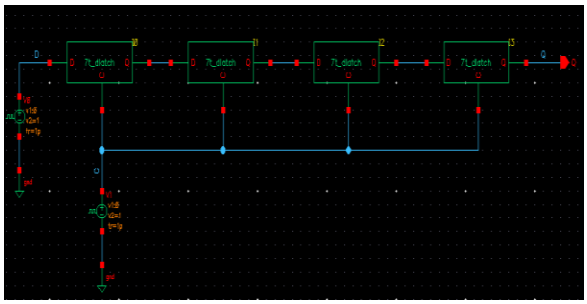

Figure 5. 7T D Latch–Based Serial-In Serial-Out Shift Register.

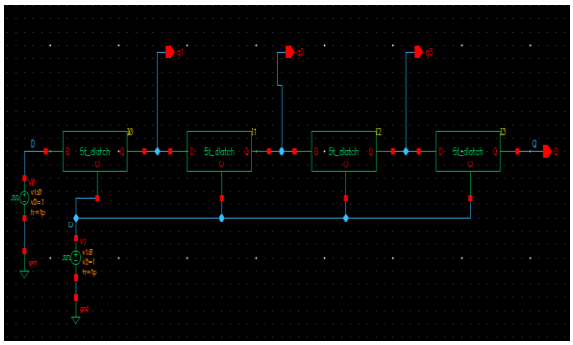

Figure 6. 5T D Latch–Based Serial-In Serial-Out Shift Register.

Figure 4, Figure 5, Figure 6 shows the schematic of 5T,6T,7T based 4-bit SISO shift register. A 4-bit Serial-In Serial-Out (SISO) register can thus be implemented using four level-sensitive D latches driven by the same clock signal. To analyze the effect of transistor overhead on power and performance, 5T, 6T, and 7T D latch-based designs of the 4-bit SISO register will thus be used. Here, the 5T-based 4-bit SISO register uses a small transistor overhead in its compact feedback path design, thus resulting in lower internal capacitance and reduced switching activity, which consumes much lower power. In contrast, for the 6T design of the register, extra transistors will be used to improve the feedback signal and achieve noise-tolerant data retention at the expense of greater power consumption and area overhead. Similarly, for the 7T design of the 4-bit register, an additional transistor will thus be used for even better data retention capabilities in the lower voltage environment. However, this will result in additional delay and overhead in the circuit. From this analysis, it can thus be concluded that while 6T and 7T designs have superior noise retention and stability performance, nevertheless the best performance in power and area will thus result in the 5T-based 4-bit Serial-In Serial-Out register design.

VII. RESULTS AND DISCUSSION

Simulations are carried out using Cadence Virtuoso in 45 nm CMOS technology with a supply voltage of 1V.

D LATCH OUTPUT

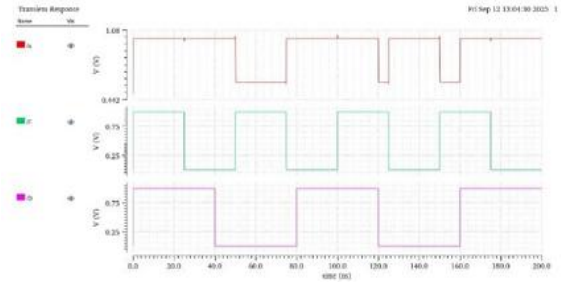

Figure 7. Output of 5T D Latch

Figure 7 denotes the transient waveform of the 5T D latch which shows that the output follows the input signal when the clock is in the active state, confirming proper data capture. When the clock switches to the inactive phase, the stored value is held steady without noticeable fluctuations in the output. The waveform obtained verifies correct latch functionality with stable operation during both the transparent and hold periods.

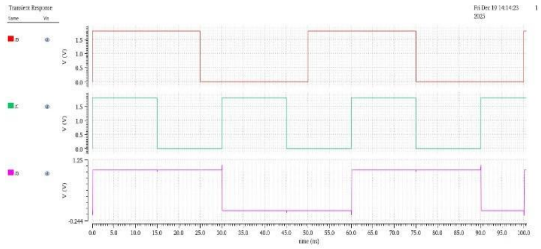

Figure 8. Output of 6T D Latch

Figure 8 denotes the simulation waveform of 6T D-latch which shows that the 6T D latch operates correctly because it restricts output movement to match input signals during the clock signal's transparent period. The output maintains a constant state when the clock stops which demonstrates that data storage functions correctly. The switching transitions show improved stability and balanced performance.

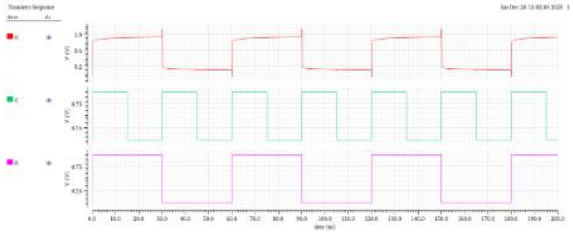

Figure 9. Output of 7T D Latch

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Figure 9 represents the transient response of the 7T D latch, showing correct data tracking when the clock is active and stable retention of data when the clock is inactive.

SISO OUTPUTS

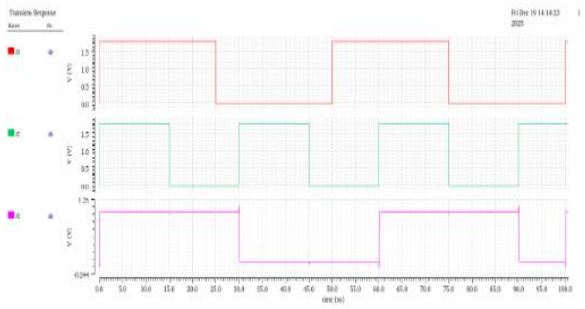

Figure 10. Transient Response of 5T D Latch Based SISO Shift Register Output.

Figure 10 waveform depicts the transient response of the 5D latch-based SISO shift register and reflects the correct serial propagation of the input data through successive clock cycles. The output waveform justifies proper data storage and shifting behavior with respect to the applied clock signal.

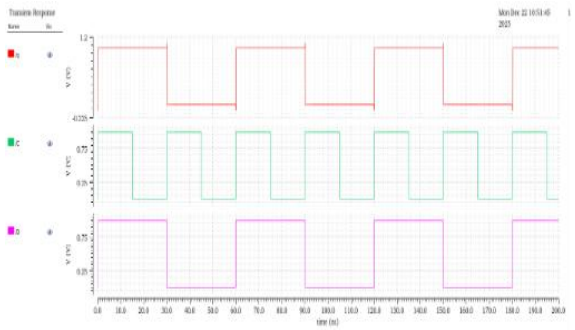

Figure 11. Transient Response of 6T D Latch Based SISO Shift Register Output.

Figure 11 represents the transient response of the 6T D latch–based SISO shift register, where the output follows the input during the active clock period and holds the data otherwise. The waveform confirms reliable serial data shifting with stable and well-defined output levels.

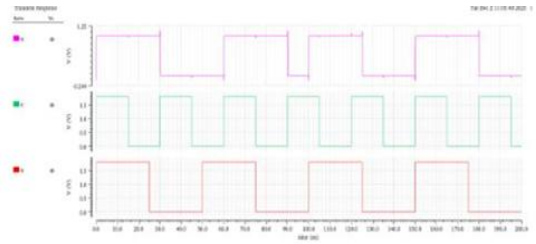

Figure 12. Transient Response of 7T D Latch Based SISO Shift Register Output.

Figure 12 represents the transient response of the 7T D latch-based SISO shift register that shows the correct serial data transfer according to the clock signal. The waveform obtained at the output signifies steady-state storage and reliable shifting with enhanced robustness and signal integrity.

Table 1. Comparison of 7T,6T and 5T D Latches

D -LATCH	POWER(W)	DELAY(s)	PDP(J)
7T	14.78×10^{-9}	21.54×10^{-12}	3.183012×10^{-19}
6T	664.8×10^{-6}	18.30×10^{-12}	1.22×10^{-14}
5T	17.43×10^{-9}	21.24×10^{-12}	3.7021×10^{-19}

The comparison between 7T, 6T, and 5T D-latch designs shows that power–delay trade-off as well as PDP variation. Although the 6T D latch shows minimum propagation delay of 18.30 ps, very poor power consumption has been observed, which results in worst PDP performance. The 7T D latch shows a low-power consumptions but a little bit higher delay compared to 6T design. In contrast, the 5T D latch maintains a low-power consumptions similar to a 7T latch. It also shows acceptable delay. Thus, it provides balanced performance among all. Hence, the 5T D latch is most suitable for low-power VLSI applications.

Table 2. Performance Comparison of 5T, 6T, and 7T D Latch–Based SISO Shift Registers (Power, Delay, and PDP)

SISO	POWER(W)	DELAY(s)	PDP(J)
7T	93.59×10^{-9}	370.4×10^{-12}	346.65×10^{-19}
6T	683.5×10^{-6}	107.7×10^{-12}	73613×10^{-19}
5T	91.38×10^{-9}	104.3×10^{-12}	95.3×10^{-19}

From the results for the comparison of the designed SISO

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shift registers Table 2 for the power consumption, delay time, and PDP by implementing 7T, 6T, and 5T D-latches, there is a huge variability in power consumption, delay time, and PDP. For the SISO shift register implemented using the 6T-latch, the value of PDP appears quite high owing to the enormously large active power consumption. Compared to the active power consumption of the 6T-latch, the active power consumption of the 7T-latch in the SISO shift register implemented using the 7T-latch is much lower; however, it involves huge delay time and thus results in a large PDP value. Owing to least active power consumption and shortest delay time, the PDP of the 5T-latched implemented SISO appears small.

VIII. CONCLUSION

In this paper, 5T, 6T, and 7T D latches have been designed and analyzed to implement low power VLSI systems. Though in standalone form, the 5T D latch PDP is slightly greater than the 7T latch, it is still much smaller than that of the 6T structure. When applied to a 4-bit Serial-In Serial-Out (SISO) shift register, it is shown that in total PDP, the 5T latch is most efficient, emphasizing their applicability in sequential circuit design. The small number of transistors in the proposed 5T structure facilitates efficient cascading to achieve speedy data transitions along with less power consumption. Hence, in conclusion, the 5T D latch is an efficient structure to be applied in SISO shift registers, achieving effective results in all aspects: speed, power consumption, and complexity.

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