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Process Corner Analysis of a Single-Ended 7t SRAM Cell at 32 NM Technology Node

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ABSTRACT

The Static Random Access Memory (SRAM) forms a crucial integrant in embedded systems. Demand for reduced power consumption has made single-ended SRAM bit-cells extremely popular. For enhanced performance of the SRAM bit-cells, the technology node scaling is prevalent to obtain increased transistor density. However, as a consequence the bit-cell undergoes various process-voltage-temperature variations are introduced during the fabrications process. Therefore, the paper studies a single-ended 7 transistor SRAM bit-cell that undergoes 1000-point Monte Carlo simulations at 0.5V VDD under 5% threshold voltage variation at various process corners to measure its read and write stability and to conclude the best and worst performing corner of the bit-cell and evaluate nominal performance values.

Keywords: SRAM cell, process corner, Monte Carlo

I. INTRODUCTION

The Static Random Access Memory (SRAM) provides as extremely integral component in any system-on-chip (Soc). With a surge in demand for high processing speed, cache memories have become highly popular. These SRAM based cache memories are formed from arrays of a single SRAM bit-cells along with peripheral devices such as sense amplifiers, write drivers and decoders. SRAM is a very common CMOS based IC and offer higher speed and reduced power consumption which caters to the growing needs of high speed computing and reduced energy utilization which is seen with continuous technological advancements in the world [1], [2], [3], [4].

The SRAM contributes to about one-third of the overall power consumption of the embedded system [5]. Hence, for reducing total consumption of power by any soc we can start with the SRAM core. Since, the characteristics of SRAM depends on the individual characteristics of the contributing bit-cells, reducing the power consumed by the bit-cell can in turn greatly reduce the overall power dissipation by the SRAM array. There can be different ways to achieve this reduction in power. One such way includes VDD (supply voltage) scaling wherein the value of operating voltage VDD of the bit-cell is decreased so as to reduce the power dissipated by the cell [6], [7]. However, this reduction in VDD supply, negatively affects the speed of performance and noise tolerance of the SRAM [8], [9], [10]. Therefore, the apt value of VDD is chosen after trade-off between the speed, power and noise tolerance so that all the parameters are satisfied with no extreme degradation in any of the parameters.

Keeping up with the Moore's Law, for increasing the transistor density of any soc, the SRAM cells also follow the trend of technology node scaling, which includes reducing the transistor sizing so as to reduce overall layout of the bit-cell area. However, the reduced technology node which has the benefits of increasing cell density comes at the expense of process-voltage-temperature (PVT) variations and increased leakage currents in the memory cells. These can degrade the readability and ability to write of the bit-cell making it tougher to perform operations on the memory cells. [11], [12], [13], [14].

Therefore, during fabrication of the SRAM cells, it is extremely important to be mindful of the PVT variations, to ensure efficient performance of the entire SRAM array. Various Monte-Carlo techniques are utilized for thorough study of these variations in the SRAM bit-cell. This Monte Carlo analysis helps observe the working of the bit-cells during write and read modes which is then used to obtain the failure probabilities and the worst case values during parametric analysis of the bit-cells [6], [15], While larger Monte Carlo samples are used to observe the worst-possible values and failure probabilities under higher process variations , reduced sample sizes can be employed under lower variation for estimation of near-nominal performance metrics with significantly less computational cost and faster analysis which is especially useful during early design stages. This approach is discussed in this work demonstrating efficient evaluation of nominal behavior under lower variation and smaller Monte Carlo sample size. This paper presents the 1000-point Monte Carlo analysis of a single bit-line 7 transistor bit-cell proposed by Bishtet al [16] with 5% variation in threshold voltages of the transistors, while performing operations such as write and read, in order to evaluate the nominal values of the parameters and successfully identifying best and worst behavior under process variations. The introduction is followed by section 2 that discusses the single-ended 7 T SRAM bit-cell, its structure and different modes of operations. Meanwhile the section 3 discusses the process corner variation and the Monte Carlo

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distribution curves and finally is followed by conclusion.

II. SINGLE-ENDED 7 TRANSISTOR SRAM CELL

Line to execute operations on the cell unlike the conventional differential-ended structures that consist of two bit-lines. Single-ended configurations are simpler and also contribute to reduced leakage currents due to reduced bit-line leakage. Figure 1 displays a single-ended 7 T SRAM bit-cell with a bistable inverter core structure [16]. The left inverter of the SRAM bit-cell consists of three transistors with the transistor acting A3 as the feedback transistor used to boost the ability to write to the bit-cell. Signal F controls transistor A3. Table 1 depicts the transistor sizing of the SRAM cell. The simulations of the cell are performed at 32 nm technology node at 0.5V VDD.

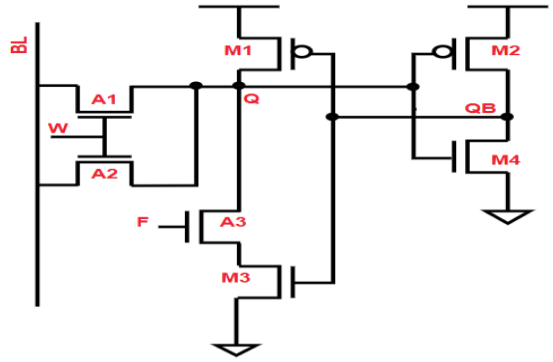

Fig 1: Structure of the single-ended 7 Transistor SRAM bit-cell

The proposed methodology focuses on creating an AI powered weather forecasting system for precision farming, integrated with an advanced, multilingual chatbot interface to provide best practice recommendations. This system uses XGBoost for machine learning techniques and LSTM for deep learning models. It integrates predictive modeling to emphasize high accuracy in weather prediction, appropriate agronomic measures, accessibility, and organized resource optimization.

TABLE I
THE W/L SIZING RATIO OF EACH TRANSISTOR THAT FORMS THE STRUCTURE OF THE DISCUSSED 7 T SRAM BIT-CELL

Transistor	W/L Ratio
M1	1
M3	4.5
M2	1
M4	2
A3	4.5
A1	3
A2	3

TABLE II
THE CONTROL SIGNALS FOR THE HOLD, WRITE AND READ OPERATIONS ON THE 7T CELL

Controls	Hold	Read	Write 0	Write 1
F	1	1	0	0
W	0	1	1	1
BL	1	1	0	1

The bit-cell performs hold, write and read operations as per the control signals shown in the given Table 2. The feedback transistor needs to be turned off during write an operation that improves performing a write-1 on the bit-cell. During hold mode, the bit-cell retains the stored value and exists in standby mode. To read the values stored by the bit-cell, read operation is executed. Meanwhile the write operation when performed is used to write values into the bit-cell, such as write-0 and write-1.

III. PROCESS CORNER ANALYSIS

The fabrication of SRAM bit-cells is susceptible to minute errors such as transistor sizing and oxide thickness, which become more evident with technology node scaling. For instance, in some cases, the PMOS may be faster than the NMOS and in some cases both PMOS and NMOS may have slower switching speeds. These variations lead to mismatch among transistors and are referred as process corner variations. The process corner mismatches severely affect the operations of the bit-cell as well as alter the output yield while influencing factors such as noise tolerance of the cell. Execution of the bit-cell while under read mode and write mode are observed under four process corners- FF i.e. Fast NMOS Fast PMOS, FS i.e. Fast NMOS Slow PMOS, SS i.e. Slow NMOS Slow PMOS and SF i.e. Slow NMOS Fast PMOS [17], [18], [19], [20], [21].

A. *Static Noise Margin*

The steadiness of cell while in standby mode and read mode is measured using the static noise margin (SNM) which gives the noise tolerance of the cell. Butterfly curve is the conventional method to measure SNM. The VTC curves of the two inverter structures of the SRAM bit-cell are plotted together which forms a two-lobed structure which is known as the butterfly curve [21], [22]. In either of the butterfly curve lobes, we embed the largest possible square shaped structure. The calculated SNM is derived using the measure of length of this maximum possible side of the embedded square. These SNM values are susceptible to PVT variations that affect the bit-cells. Hence, a 1000-point Monte Carlo analysis can be performed wherein the threshold voltage (VTH) is varied by 5% of the nominal values under the four process corners. There 3-σ distribution curves are displayed in Fig.2.

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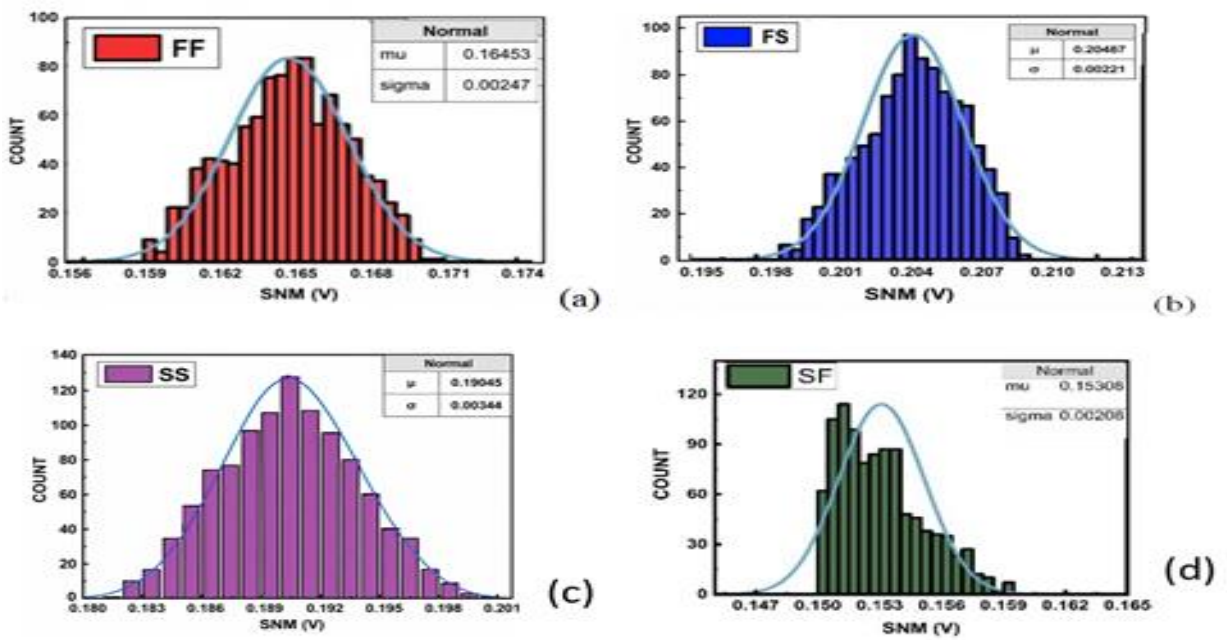

Fig. 2. The Gaussian distribution curves for SNM obtained after Monte Carlo runs at (a) FF, (b) FS, (c) SS and (d) SF process corner

The mean values of SNM obtained under FF, FS, SS and SF corners are calculated as 0.164 V, 0.204 V, 0.19 V and 0.153 V respectively. The best performance can be seen at FS process corner while the SF corner serves as the worst performing process corner.

B. Write Margin

Performing a write on the cell is most challenging to achieve as during write operation, the bit-cell is highly susceptible to noise and can easily register an incorrect flip in the value retained by the cell. Therefore, the parameter write margin is used to measure the ability to write to a cell. In order to calculate the write margin, we first measure the parameter known as write trip point (WTP) of any bit-cell [23], [24]. WTP measures the least value of the bit-line voltage that can register an incorrect inversion in the content retained in the cell. Once the WTP is obtained, we can easily measure the write margin, which is the value of difference in values of the VDD and WTP.

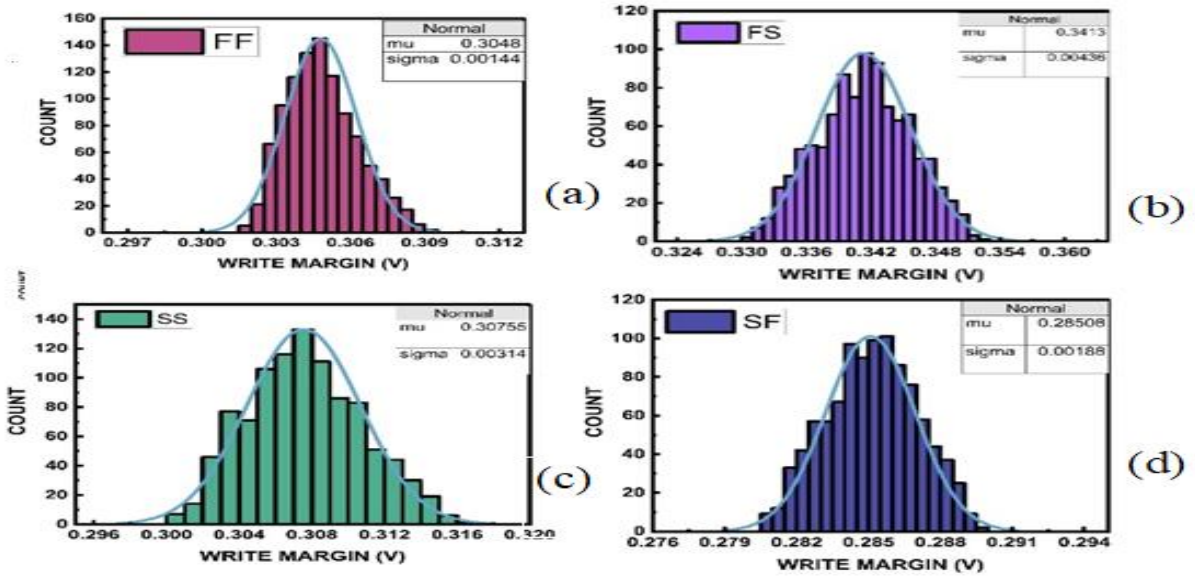

Fig. 3. The Gaussian distribution curves for write margin obtained after Monte Carlo runs at (a) FF, (b) FS, (c) SS and (d) SF process corner

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1000-point Monte Carlo runs were performed on the bit-cell at VDD of 0.5 V, at all four process corners with a 5% variation in VTH and the values of write margins thus obtained are then used to plot the 3-σ Gaussian distribution curves as displayed in Fig. 3. The mean write margin obtained at process corners named as FF, FS, SS, and SF are 0.304 V, 0.341, 0.307 V and 0.285 V respectively.

It is successfully evaluated that best execution of the bit-cell is displayed at FS corner while SF serves as the worst performing process corner. This can arise because at SF corner the weaker NMOS finds it difficult to hold the logic '0' during read operation and performing write-0 operations. As a result, the cell is more vulnerable to noise for longer period of time and can suffer from unexpected erroneous flips during the operations therefore making the SF corner as the worst performing process corner [25]. The observation remains consistent with prior studies [16] regarding the behavior of the cell under different process corners and the concluding trends were prevalent even under reduced sample sizes and hence a reduced computational cost.

IV. CONCLUSION

Technology node scaling has resulted in greatly enhancing the cell density of the SRAM array however, as a consequence, given rise to mismatch in the form of PVT variations which arise during fabrication process and severely affect the cell performances while performing the hold, write and read operations. Thus, it is important to study these variations. Hence, the Monte Carlo runs approach is used so as to plot the Gaussian distribution curves and observe the worst performing variation as well as the mean values and standard deviation of the SNM and also the write margin. The sample size is reduced and evaluated under lower variation in the threshold voltage at different corners so as to successfully evaluate nominal values with decreased computational cost and faster processing, which is especially useful during early design stages. The process corner mismatch then is further studied for four different corners namely FF, FS, SS and SF corners. The distribution plots for the four process corners are obtained for SNM and write margin to measure the noise tolerance during performance of write and read operations. The analysis thus gave the observation that the 7 Transistor bit-cell discussed, performs best under the FS process corner and worst at SF corner.

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