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Comparative Power–Delay–HSNM Analysis of a 7T SRAM Cell at 45 nm, 32 nm, and 22 nm

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ABSTRACT

This paper describes the detailed performance study of a low power, single ended 7T SRAM cell across various technological nodes of 45nm, 32nm, and 22nm. The best result of power dissipation is obtained at the technology node of the 32 nm process for this SRAM cell, where the powers of Write 1, Write 0, Read 1, and Read 0 operations are measured as 0.4523 (µW), 0.778 (µW), 0.259 (µW), and 0.418 (µW), respectively. Additionally, this cell shows better delay performance at the technology node of the 32 nm process, where the Write1, Write0, and Read0 delay times are measured as 18.13 ps, 14.7 ps, and 15.6 ps, respectively, to enable the memory access process faster. Moreover, the single ended 7T SRAM cell shows the highest noise margin at the technology node of the 32 nm process compared to the other two processes, where the highest noise margin value measured at the technology node of the process is 0.32807 V, as opposed to values of 0.30184 V and 0.26861 V at the technology nodes of the other two processes, respectively.

Keywords: Single ended, SRAM, HSNM, low power,

I. INTRODUCTION

High-density and stable SRAMs are required for advanced digital systems, and this largely influences the overall power dissipation [1]. The embedded memories of microprocessor-based systems consume a substantial part of the SoC, hence the need for low power memory in battery-driven applications. In continuous CMOS scaling, the challenges in SRAM cell design have progressively become power, delay and stability, especially at low supply voltages. Voltage scaling allows circuits to be designed to work in the sub threshold region [3]. This is done with the objective of reducing the power consumption of circuits by a large amount with an exponential decrease in performance [4]. But there are certain challenges involved in using voltage scaling to design VLSI circuits. These include a low static noise margin (SNM), a range of values for the currents due to PVT variability, as well as a constraint the number of cells per bitline [5-6]. Due to such challenges, a 6T SRAM cell will not be able to work with a low voltage. This paper presents a single ended 7T SRAM cell design, where stacked transistors and feedback control signals improve the stability and reduce power consumption without any external assist circuitry [7]. In the read operation, the SRAM cell transfers the stored data to the bit line while maintaining data integrity [8]. The bit-line in an SRAM cell is used to read data from or write data to the cell, acting as the communication path between the cell and peripheral circuitry. These constraints make it difficult for ordinary six-transistor (6T) SRAM cells to function consistently with low-voltage power supplies [9].make it difficult for ordinary six-transistor (6T) SRAM cells to function consistently with low-voltage power supplies [11].

In this paper cell, the SRAM cell is evaluated at 45nm, 32nm, and 22nm technology node for power, delay, hold static noise margin, and area. Simulation results demonstrate that the 32nm node has the greatest trade-off among lower power, balanced delay, highest HSNM, allowing its suitability for low power applications.

II. SCHEMATIC DESIGN

The single ended 7T SRAM cell consists of a cross-coupled inverter pair, where the left inverter is implemented by three cascaded transistors. In hold mode, data is stored through two series connected cross-coupled inverter paths: P1-P3-P4 and P2-P5. One NMOS transistor is controlled by write word-line, which provides data transfer between storage

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node Q and one single bitline (BL). At read cycle, the read word-line is asserted, and the stored data can be sensed on the same bit line. A column-bias-based feedback control signal is required to drive the feedback-cutting transistor P3, which significantly improves the stability during write operation.

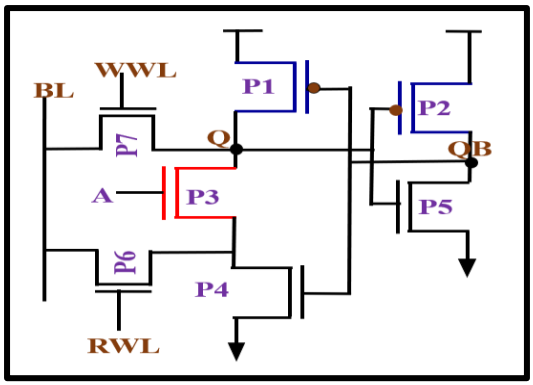

Fig.1 Schematic design single ended 7T SRAM cell

A. Hold operation:

In the single ended 7T SRAM cell, the retention of the data in hold mode is provided through a stacked-cross-coupled inverter. The cell has only one cross-coupled inverter pair, in which the left inverter is implemented using three stacked transistors, whereas the complementary inverter is implemented using two transistors. In the hold phase, both write word lines are kept inactive, and the feedback control signal A is held at a high level, which enables transistor P3, thus providing very strong feedback between the two internal nodes. This facilitates the two stacked inverters (P4-P3-P1 and P2-P5) to provide better retention of the stored data.

B. HSNM

The Hold Static Noise Margin (HSNM) is the worst-case allowable DC noise voltage that the SRAM cell can tolerate when in the hold mode without upsetting the stored data, and it signifies the stability of the SRAM cell. With the HSNM values, the result shows that the HSNM for this SRAM cell increases from as shown in Figure 2-4 the HSNM is 0.30184V at 45nm to 0.32807V at 32nm. However, it decreases to 0.26861V at 22nm because the leakage currents are pronounced when the technology node scales to the smaller size. Among the technology nodes that have been tested, the result confirms that this SRAM cell is the most stable at the 32nm node. Thus, the most stable technology node for the hold operation is 32nm.

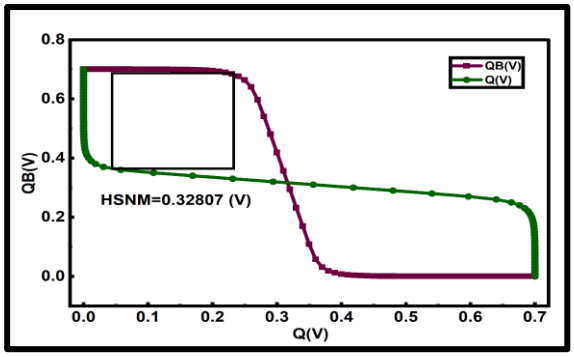

Fig.2 HSNM at 32nm

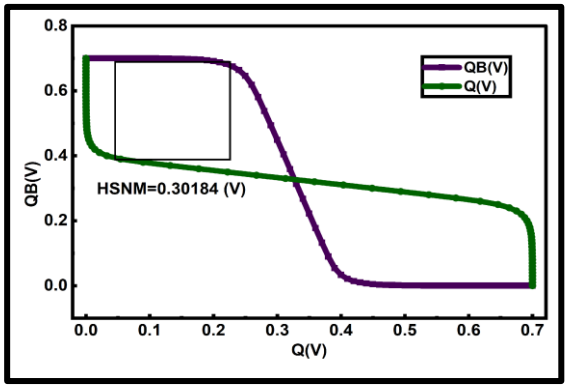

Fig.3 HSNM at 45nm

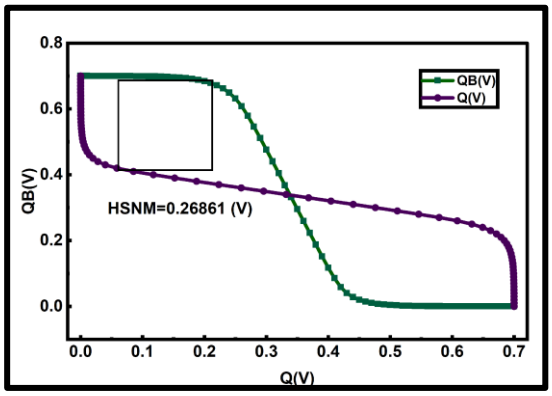

Fig.4 HSNM at 22nm

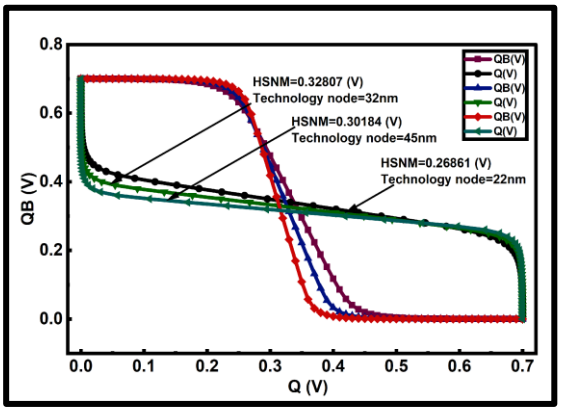

Fig.5 HSNM at 32nm 45nm 22nm

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C. Read operation

In the read operation, bit line (BL) is precharged to VDD, and read word line (RWL) is turned ON, while write word line (WWL) is kept LOW. Since QB holds logic '1,' transistor P4 is turned ON, providing a path to BL through which current can discharge BL, which is then sensed by a full-swing inverter sense amplifier. Since WWL is LOW, node Q is isolated during read, which reduces the probability of read errors based on process variability. In figure 6 shows the read-0 operation.

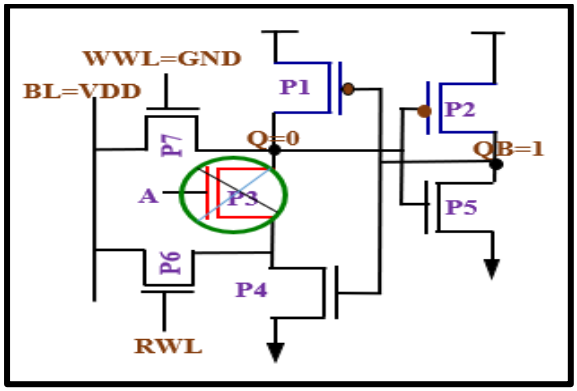

Fig.6 Read-0 operation

D. Write operation

In this paper, this 7T SRAM cell has been evaluated across the 22 nm, 32 nm, and 45 nm technology nodes to explore its write performance and scalability. The cell improves write-ability by weakening the pull-down path through transistor P3, thus allowing for reliable write operations with no boosted supply or external assist circuits. During the write '1' shows in Figure 7, A is kept low in order to turn OFF P3, allowing node Q to be completely charged through the bit-line when WWL is asserted, as the feedback path is cut. During the write '0' shows in Figure 8, A, WWL, and RWL are enabled, providing a strong discharge path through P6 and access transistor P7, balancing the write speed of both the logic states for a common write pulse width. Among the three modes evaluated, the 7T cell shows outstanding performance at 32 nm due to the proper balance between drive strength, leakage, and process variability, thereby enhancing write margin and ultra-low-voltage operation stability. Further, widening the width of P7 to 2× enhances the write current, thus assuring strong write performance across all the three nodes.

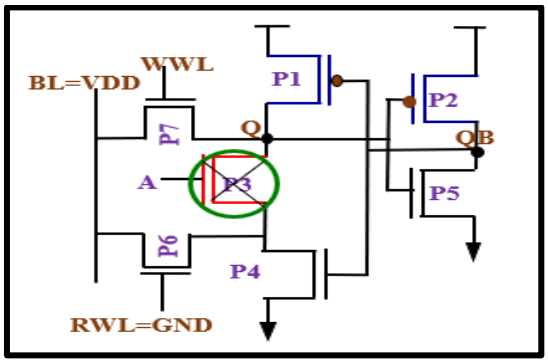

Fig.7 Write-1 operation

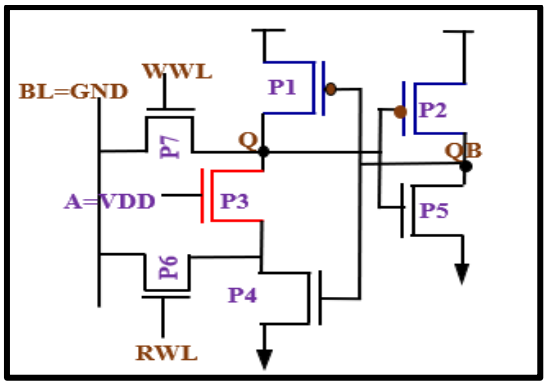

Fig.8 Write-0 operation

III. POWER CONSUMPTION

This 7T SRAM cell power behavior is validated at 45nm, 32nm, and 22nm technology nodes for both read and write modes. In the 45nm process node, the cell dissipates more power under the write-1 operation compared to other modes, reflecting higher switching activity at this node. The write 1 and write-0 modes, which are 0.9145 (µW) and 1.25 (µW), respectively, at 0.7V, and for the read-1 and read-0 modes, which are 0.453(µW) and 0.603 (µW), respectively. The 32nm technology node consumes the least amount of power for all the technologies, which are 0.4523 for write-1, 0.778 (µW) for write-0, 0.259 (µW) for read-1, and 0.418 (µW) at 0.7V for the read-0 mode, respectively. The 7T SRAM cell consumes more power (write-1: 0.6012 (µW), write-0: 0.897 (µW), read-1: 0.358 (µW), read-0: 0.576 (µW) at 0.7V for 22nm technology node compared to 45nm; thus, it shows higher power compared to 32nm owing to the penalty of leakage for deeper scaling as shown in Figure 13. This cell exhibits more power consumption at the 32nm technology node; therefore, it is the most preferable technology node for low-power consumption applications.

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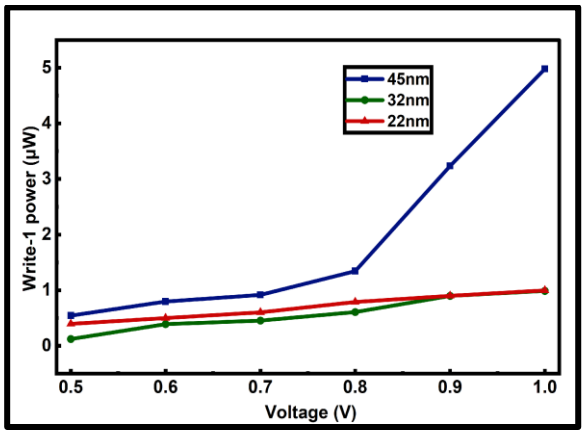

Fig.9 Write-1 power at different voltages

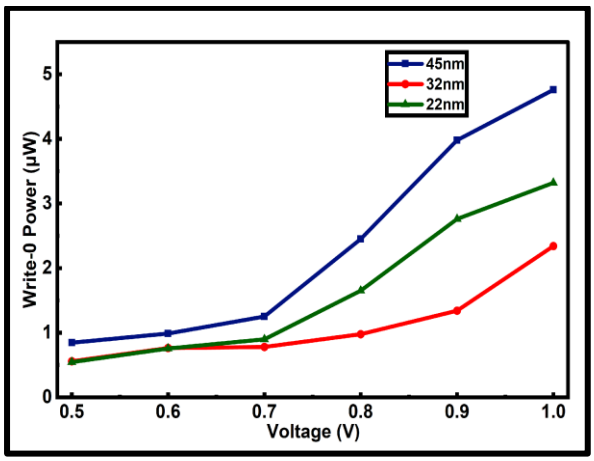

Fig.10 Write-0 power at different voltages

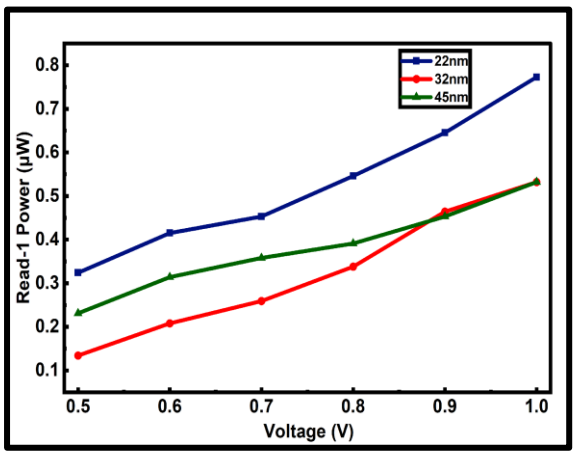

Fig.11 Read-1 power at different voltages

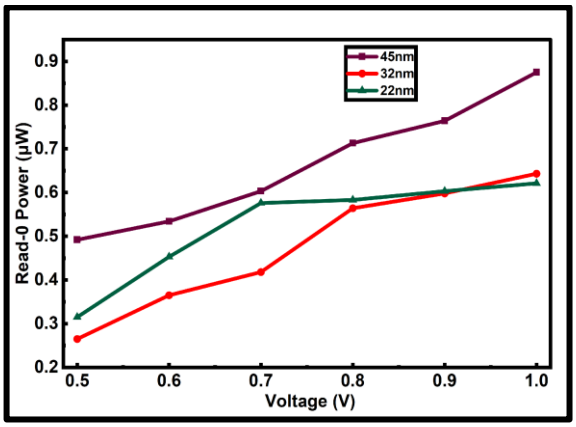

Fig.12 Read-0 power at different voltages

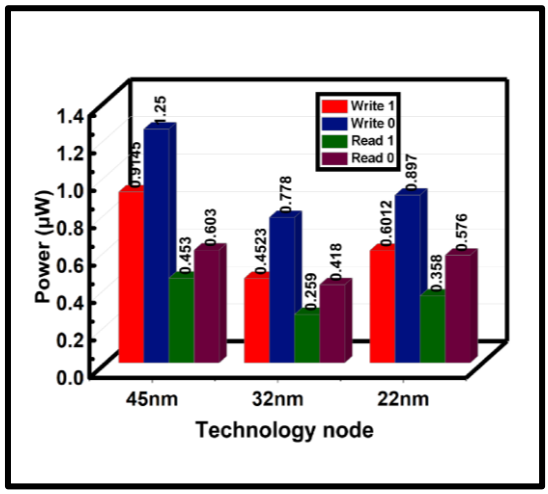

Fig.13 Power at 45nm 32nm 22nm at 0.7V

IV. DELAY

Delay is the time taken by the SRAM cell to successfully complete the write or read operation and directly affects the memory access speed. The delay performance of this 7T SRAM cell is calculated for 45 nm, 32 nm, and 22 nm technology processes. On the 45 nm process, the write-1 delay of 11.3 ps, a write-0 delay of 38.76 ps, and a read-0 delay of 39.81 ps. The new technology of the 32 nm process shows better and balanced delay performance compared to the previous one, taking a write-1 delay of 18.13 ps, a write-0 delay of 14.7 ps, and a read-0 delay of 15.6 ps. In contrast to this, the 22 nm node gives the values of write-1, write-0, and read-0 delays as 14.3 ps, 29.4 ps, and 36.19 ps at 0.7V. On the whole, the most optimal delay performance in the 32 nm node is offered by the 7T SRAM cell.

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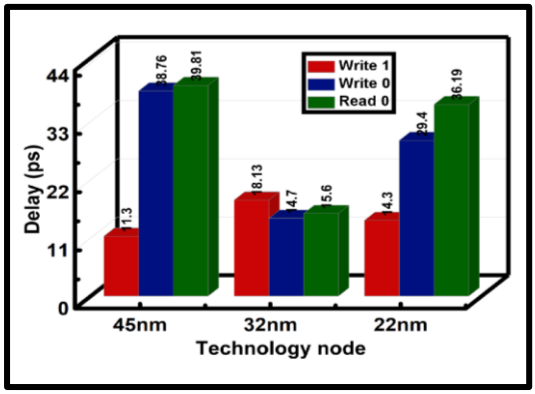

Fig.14 Delay at 45nm 32nm 22nm

TABLE 1: COMPARISON TABLE POWER

	POWER (µW)			
Technology node	Read-0	Read-1	Write-1	Write-0
45nm	0.603	0.453	0.9145	1.25
32nm	0.418	0.259	0.4523	0.778
22nm	0.576	0.358	0.6012	0.897

TABLE 2: COMPARISON TABLE DELAY

	DELAY (PS)		
Technology node	Read-0	Write-0	Write-1
45nm	39.81	38.76	11.3
32nm	15.6	14.7	18.13
22nm	14.3	29.4	14.3

TABLE 3: Table of HSNM (V)

TECHNOLOGY NODE	HSNM (V)
45NM	0.30184
32NM	0.32807
22NM	0.26861

V. CONCLUSION

The proposed 7T SRAM cell represents the optimum performance at the 32 nm technology node based on its power, delay, and stability analyses. The power consumptions in 32 nm are at the lowest for all the operations: the write-1 power is 0.4523 (µW), the write-0 power is 0.778 (µW), the read-1 power is 0.259 (µW), and the read-0 power is 0.418 (µW) shows in table 1, which is far less compared to 45 nm and 22 nm. Similarly, the delay is excellent and well-balanced at 32 nm-write-1 is 18.13 ps, write-0 is 14.7 ps, and read-0 is 15.6 ps-which ensures that the memory access will be faster and more efficient that shows in table 2. The stability of the cell also comes out to be maximum at 32 nm because HSNM at 32 nm is having the highest value of 0.32807 V compared to 0.30184 V at 45 nm and 0.26861 V at 22 nm as shows in table 3. Altogether, the overall simultaneous enhancements of the two factors, power efficiency, and speed with respect to noise stability support the view that 32 nm technology is the most viable alternative for the proposed 7T SRAM cell because it ensures the best trade-off solution.

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REFERENCES

[1] K. Roy, S. Prasad, Low Power CMOS VLSI Circuit Design, 1st edn. (Wiley, New York, 2000), ISBN: 978-0-471-11488-8

March 2000, 376 pages

[2] E. Seevinck, F. J. List, and J. Lohstroh, "Static-Noise Margin Analysis of MOS SRAM Cells," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 5, pp. 748–754, Oct. 1987, DOI: 10.1109/JSSC.1987.1052809

[3] A. Wang, A. Chandrakasan, A 180-mV subthreshold FFT processor using a minimum energy design methodology. IEEE J. Solid-State Circuits 40(1), 310–319 (2005), DOI: 10.1109/JSSC.2004.837945

ISBN: 978-81-985770-0-9

[4] A. Bhavnagarwala, X. Tang, J. Meindl, The impact of intrinsic device fluctuations on CMOS SRAM cell stability. IEEE J. Solid-State Circuits 36(4), 658–665 (2001), DOI: 10.1109/4.913744

[5] B. Cheng, S. Roy, A. Asenov, The impact of random doping effects on CMOS SRAM cell, in Proceedings 30th European Solid-State Circuits Conference (ESSCIRC), Belgium, pp. 219–222, 2004, DOI: 10.1109/ESSCIR.2004.1356657

[6] R. Gonzalez, B. Gordon, M. Horowitz, Supply and threshold voltage scaling for low power CMOS. IEEE J. Solid-State Circuits 32(8), 1210–1216 (1997), DOI: 0018-9200(97)05302-X.

[7] B. Rawat and P. Mittal, "A low-power single bit-line configuration-dependent 7T SRAM bit cell with process-variation tolerant enhanced read performance," Analog Integrated Circuits and Signal Processing, vol. 115, pp. 77–92, 2023, DOI: 10.1007/s10470-023-02147-x.

[8] C.-H. Lo, S.-Y. Huang, P–P–N based 10T SRAM cell for low-leakage and resilient subthreshold operation. IEEE J. Solid-State Circuits 46(3), 695–704 (2011), DOI: 10.1109/JSSC.2010.2102571

[9] D. Markovic, C.C. Wang, L.P. Alarcon, T.-T. Liu, J.M.Rabaey, Ultralow-power design in the near-threshold region. Proc. IEEE 98(2), 237–252 (2010), DOI: 10.1109/JPROC.2009.2035453

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