AOI :10.100.234513.0252
13th international conference on Microelectronics, Circuits and Systems, Micro2026

A Nano-Power Cascoded β-multiplier CMOS Voltage Reference with -90 dB PSRR 0.00085%/V Line Sensitivity

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ABSTRACT

This paper presents a nano-power cascoded β-multiplier CMOS Voltage Reference without the use of passive filters. The circuit includes a start-up, output stage, β-multiplier circuit, bias current generator, and operational amplifier to achieve a high-power supply rejection ratio and low line sensitivity. The cascoded β-multiplier CMOS Voltage Reference is implemented on 180 nm of technology. The reference voltage is 430.23 mV operating from a wide supply range of 0.9 V to 3.0 V. The Power Supply Rejection Ratio is -90.86 dB at 1 kHz, and the line Sensitivity is 0.0008 %/V. Furthermore, the design achieves an ultra-diminished power consumption of only 379.16 nW, with a total output noise of 27.17 nV/√Hz and draws a mere 421.29nA of supply current at 0.9V. The measured TC was found to be 58.2 ppm/°C.

Keywords: Beta-Multiplier, Power Supply Rejection Ratio, Line Sensitivity, ultra-low power consumption, Temperature Coefficient

I. INTRODUCTION

Voltage references are crucial components in integrated circuits (ICs), providing stable voltage levels essential for the precise operation of analogue and mixed-signal systems. These systems require consistent performance despite varying environmental conditions, power supply fluctuations, and semiconductor process deviations. This demanding requirement for consistency is particularly critical in power-sensitive domains like IoT devices, medical implants, and portable electronics, where both reliability and efficiency are essential [1]. Most references achieve this temperature-invariance by combining two types of currents: Proportional to Absolute Temperature (PTAT) and Complementary to Absolute Temperature (CTAT) [2]. In most System-on-a-Chip (SoC) designs, achieving an immunity to temperature changes, supply voltage, process, and mismatch variations is a main requirement, which makes the voltage reference an ideal fit [3]. Consequently, they are essential components in multiple analogue circuit applications, including Analog-to-Digital Converter (ADCs), power management systems, linear regulators, sensors, IoT, and wearable devices [4]. Numerous CMOS voltage reference designs in recent years are targeting low power and improved output stability, [5]– [16] have achieved either low power or good output stability. In [5], the proposed design is optimised for low-voltage mixed-signal applications, offering improved line sensitivity and moderate temperature stability. However, its ability to drive heavy loads comes at the expense of significantly elevated-power consumption, low PSRR and degraded performance. Another beta-multiplier-based reference is introduced in [6], a CMOS voltage reference is presented that utilises a hybrid combination of both 1.2 V and 3.3 V NMOS transistor to achieve temperature compensation via threshold voltage subtraction. The design incorporates a Beta-multiplier and an active operational amplifier to obtain a high PSRR and a low mean temperature coefficient. However, the inclusion of an active operational amplifier and multiple high-voltage transistors increase the power consumption. In [7], a subthreshold CMOS voltage reference is presented that utilises a piecewise curvature compensation technique to achieve an ultra-diminished power consumption and diminished temperature coefficient (TC). However, this design relies on the use of high-threshold transistors, which complicates the fabrication process and requires specific CMOS nodes. In [8], a self-biased current source with a stacked diode-connected MOS structure is introduced, yielding 15.4 nW consumption and low process sensitivity. However, this emphasis on process compensation comes at the cost of line sensitivity and noise performance with a modest PSSR. A PTAT-embedded amplifier is employed in [9], which combines the gate-source voltage of different-threshold NMOS pairs with a resistor-scale PTAT voltage to maintain low power consumption and high PSRR, but the circuit relies on large passive resistors, which consume significant silicon area and increase noise. In [10], a threshold-difference-based reference achieves the lowest power consumption among the compared literature without using resistors or amplifiers. However, this extreme reduction in power and complexity results in a poor PSRR. A multi-output stacked architecture is proposed in [11], generating three simultaneous voltages, using a triple-stage stacked diode-connected load, with ultra-low power, but requires at least 1.2V of supply voltage and exhibits a poor line sensitivity. In [12], a compact dual-output reference with cascode current mirrors achieves a strong PSRR, but a higher power consumption compared to simpler single-output subthreshold designs.

In [13], curvature correction currents derived from subthreshold leakage are combined with PTAT and CTAT voltages to generate a stable reference with robust PSRR with low-voltage threshold (LVT) transistors, but the design consumes significantly higher power, and LS

978-81-689089-0-1

remains sensitive to process variations. [14] is a resistor-less MOSFET-based reference integrated with current-subtraction compensation to extend operation up to 200°C, achieving low TC. While the elimination of resistors significantly reduces the active area, it results in very high-power consumption with poor PSRR. In [15], nanowatt bandgap and sub-bandgap references eliminate passive resistors through cascaded MOS differential pairs, reducing power and area but suffering from high temperature coefficients and increased complexity. In [16], an ultra-compact all-MOS reference design achieves remarkable precision through high-order temperature compensation without resistors or amplifiers, resulting in small area consumption. However, it struggles with poor line sensitivity and poor load driving capability. Refer Table 2. For Comparison of current state of the art.

Hence, with respect to the suggested literature, it is observed that the trade-off between the power consumption and line sensitivity, PSRR and noise is hard to achieve. It was also noted that the use of cascode current mirrors improves the PSRR significantly. Thus, while keeping the above literature in consideration, this paper presents a nano-power cascoded β-multiplier CMOS voltage reference (CBCVR) designed to address the trade-off between low-power efficiency and stability, i.e., with regards to good line sensitivity, low noise and high PSRR. The proposed circuit is mostly related to [5] and [6]. To overcome the limitations in previous works, stabilisation by cascading the PMOS current mirrors and amplifier-feedback techniques is introduced. Additionally, the proposed CBCVR design aims to enhance the noise performance without using any passive R-C filters and intends to utilise only standard, typical MOSFETs instead of using MOSFETs with a different threshold value to avoid complicating the fabrication process

The work is divided into four sections. Section II provides a detailed analysis of the proposed design and architecture, outlining the circuit's working principles and stabilisation mechanisms. Section III discusses the post-simulation results and performance metrics, including reference voltage stability, line sensitivity, noise performance, PSRR, power consumption, and temperature compensation. Finally, Section IV concludes the paper and summarises the primary contributions of this work.

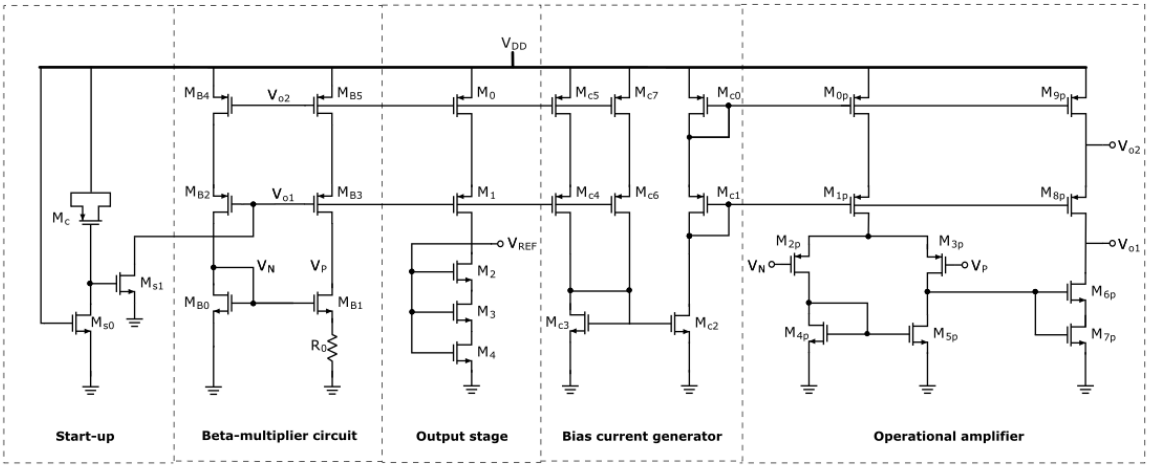

Fig. 1 Circuit of the Proposed CBCVR

II. DISCUSSION OF THE PROPOSED CBCVR

The suggested CBCVR's primary architecture is depicted in Fig. 1. The startup circuit, the operational amplifier, the output stage, the bias current generator, and the beta-multiplier circuit are the components that comprise the high PSRR voltage reference circuit. This circuit is designed for low-power operation.

A. Start-up circuit

The general idea of the start-up circuit was referenced by [7]. The implementation of the start-up circuit comprises transistors M_{s0}, M_{s1} and M_C, where M_C is utilised as the MOS capacitance, ensuring that the main circuit doesn't get stuck in a zero current state. The transistors M_{s0} and M_{s1} act as the NMOS switch, while the M_C acts as a storing element, ensuring the effective switching function. The drain potential of M_{s0} or the source of M_{s1} is initially low. As the gate of M_{s0} is high, M_{s0} is ON and pulls the source of M_{s1} towards the ground. As long as the gate potential of the M_{B4} and M_{B5} remains high, the PMOS current mirrors are OFF. Hence, a low voltage is sensed at the source of M_{s1}, which then turns On and starts pulling the gate potentials of M_{B4} & M_{B5} towards the ground, creating a pull-down effect. This results in activation of the PMOS current mirrors (M_{B4}, M_{B5}, M_{B2}, M_{B3}), drawing current into the reference core. The main reference loop then backs up the pulled-down voltage to the correct bias voltage for normal operation. The start-up then deactivates as the source-gate voltage of M_{s1} drops, turning M_{s1} OFF. The aspect ratios of all transistors utilised are summarised in Table 1.

978-81-689089-0-1

TABLE 2
TRANSISTOR SIZING UTILISED IN THE ARCHITECTURE

Transistor	W/L(μm/μm)	Transistor	W/L(μm/μm)
M1, M0	8/1	M4	0.97/0/.18
M2	1.05/1	M3	0.85/0.18
MB1	1.5/1	Mc2	0.5/1
MB3,MB2, MB5, MB4, Mc, M2p, M3p, M1p, M8p,Mc1, Mc4,Mc6, M0p,M9p, Mc0,Mc5, Mc7,M6p, M7p	2/1	M4p,M5p, Mc3,MB0, Ms1, Ms0	1/1

B. Beta Multiplier Circuit

The function of a Beta Multiplier in this circuitry is to establish a stable, well-defined current, i.e. $I_{REF,}$ which is independent of power supply variation due to the cascode current mirror. And to establish this non-zero, stable current, the core circuit comprises transistors M_{B2}, M_{B3}, M_{B4} and M_{B5} that form a cascode current mirror pair. Where the M_{B2} and M_{B3} form the basic PMOS current mirror pair with the same aspect ratio and also the same gate-source voltage, which enforces $I_{D2} = I_{D3,}$ i.e. is the current flowing through M_{B2} and M_{B3}, respectively. These NMOS transistors would be operating in the subthreshold region in the case when gate to source potential is lower than threshold voltage and $I_{DS,}$ i.e. the applied drain to source conduction current, is really low but not zero. The current in the subthreshold region [14] would be expressed as:

$$I_{DS} = \mu C_{ox} \frac{W}{L} (\eta - 1) V_T^2 \, exp \, exp \left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \quad (1)$$

Where the C_{ox} stands for oxide capacitance, μ denote carrier mobility, W represents the channel width, L represents channel length, and the η is a non-ideality factor. The above expression (1) can also be simplified as

$$I = I_{DS} = \frac{W}{L} I_0 \, exp \, exp \left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \quad (2)$$

where $I_0 = \mu C_{ox} (\eta - 1) V_T^2$

The output of the high-gain amplifier drives the gate of the PMOS current mirror pair that acts as a control voltage V_{o1}. Then there are transistors M_{B4} and M_{B5} that form the cascode stage, and their gates are connected to $V_{o2,}$ which is another bias voltage provided by the amplifier. The transistors M_{B4} and M_{B5} increase the output impedance of current mirror, causing the currents I_{D2} and I_{D3} to be way less sensitive to the variations in their drain voltages, i.e. node V_N and $V_{P,}$ respectively. This helps in significantly improving the PSRR. Hence, the result of cascode mirror ensures that the current flowing down M_{B1}/ R_0 branch (I_{D1}) and the current flowing down the M_{B0} branch (I_{D0}) are identical, i.e. $I_{D0} = I_{D1}$. Followed by the cascode current mirrors, the NMOS transistors M_{B0} and $M_{B1,}$ with their grounded sources and their gates are connected to V_N and $V_{P,}$ respectively. The gate to source potential of transistors M_{B0} and M_{B1} can be stated by using (2) as V_{GS1} and $V_{GS0,}$ respectively.

$$V_{GS0} = V_{TH} + \eta V_T \; ln \, ln \left(\frac{I}{I_0 \, S_{B0}}\right) \quad (3)$$

$$V_{GS1} = V_{TH} + \eta V_T \; ln \, ln \left(\frac{I}{I_0 \, S_{B1}}\right) \quad (4)$$

Where S_{B0} and S_{B1} denote its aspect ratios, i.e. W/L ratios of transistors M_{B0} & $M_{B1,}$ respectively. The voltage across R_0 of value 440kΩ i.e. $V_{R0,}$ is typically set by their difference in V_{GS} to create a PTAT current which can be equated as

$$V_{R0} = V_{GS0} - V_{GS1} \quad (5)$$

By using (3) & (4), the above equation can be stated as

$$V_{R0} = \eta V_T \left[ln \, ln \left(\frac{I}{I_0 \, S_{B0}}\right) - ln \, ln \left(\frac{I}{I_0 \, S_{B1}}\right)\right]$$

$$V_{R0} = \eta V_T \; ln \, ln \left(\frac{S_{B1}}{S_{B0}}\right) \quad (6)$$

The voltage drop across R_0 is established by the difference in gate source voltages of the main mirror transistors. For the voltage reference to be stable, V_P must be equal to $V_{N,}$ i.e. $V_P = V_{N,}$ which is held true by the NMOS devices by enforcing $V_{GS1} = V_{GS0}$. The stable reference current is then established when the currents I_{D0} and I_{D1} satisfy the voltage feedback constraint $V_P = V_N$, setting the current I flowing through the entire structure, which is evaluated through the resistor R_0 as

$$I = \frac{V_R}{R_0} = \frac{\eta V_T}{R_0} \; ln \, ln \left(\frac{S_{B1}}{S_{B0}}\right) \quad (7)$$

C. Output Stage

This stage uses a combination of PMOS and NMOS transistors to generate a stable bias voltage, i.e. V_{REF}. The PMOS transistors M_0 and $M_{1,}$ with their gates connected to the bias voltages V_{o2} and $V_{o1,}$ respectively, form a cascoded current mirror load for the NMOS stack. And since the V_{o2} and V_{o1} are common to the other current mirrors, ensure that the current flowing through output branch (I_{REF}) is mirrored to main current reference circuitry. This cascode configuration of M_0 and M_1 provides a high output impedance, making the output current highly stable and less susceptible to variations in the voltage at the drain of M_0 or at the drain of M_1. Then there are three series-connected, i.e. with their gate connected to drain NMOS transistors M_2, M_3 and $M_{4,}$ which serve as a high impedance load and voltage setting stack. The total voltage drops across this stack determines the voltage at the output node, V_{REF}. By stacking multiple gate-source voltages, the voltage reference circuit can generate a voltage, V_{REF} and thus can have a predictable TC, which can be stated as:

$$V_{REF} = V_{DS2} + V_{DS3} + V_{DS4} \quad (8)$$

Where V_{DS2}, V_{DS3} and V_{DS4} represent the respective drain to source potential of the transistors M_2, M_3 & M_4. V_{DS2} can be expressed as

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$$V_{GS2} = V_{DS2} = V_{TH} + \eta V_T \ ln\ ln\ (\frac{I}{I_0\ S_2}) \quad (9)$$

Where the gate to the source potential of M_2 is denoted by V_{GS2} and S_2 denotes the respective aspect ratio of transistor M_2. Similarly, the gate to source potential V_{GS3} and V_{GS4} of transistors M_3 & M_4, respectively, can be equated as

$$V_{GS3} = V_{REF} - V_{DS4}\ ; V_{GS4} = V_{REF} \quad (10)$$

Considering equations (8) and (10), V_{GS3} could be modified as

$$V_{GS3} = V_{DS2} + V_{DS3} = V_{REF} - V_{DS4} \quad (11)$$

The expression of V_{DS3} can be equated using (9) and (11) as

$$V_{DS3} = V_{GS3} - V_{DS2} \quad (12)$$

$$V_{DS3} = V_{TH} + \eta V_T \ ln\ ln\ (\frac{I}{I_0\ S_3}) - V_{DS2}$$

Substitute the value of V_{DS2} from (9)

$$V_{DS3} = \eta V_T \ ln\ ln\ (\frac{S_2}{S_3}) \quad (13)$$

Where S_3 signifies the aspect ratio of transistor M_3. Similarly, the expression of V_{DS4} can be stated using (10) as

$$V_{DS4} = V_{GS4} - V_{GS3} \quad (14)$$

$$V_{DS4} = \left[V_{TH} + \eta V_T \ ln\ ln\ \left(\frac{I}{I_0\ S_4}\right)\right] - \left[V_{TH} + \eta V_T \ ln\ ln\ \left(\frac{I}{I_0\ S_3}\right)\right]$$

$$V_{DS4} = \eta V_T \ ln\ ln\ (\frac{S_3}{S_4}) \quad (15)$$

Where S_4 signifies the aspect ratio of M_4 transistor. Now equating values of V_{DS2}, V_{DS3} and V_{DS4} from (9), (13) and (15) respectively in equation (8), the output V_{REF} is expressed as

$$V_{REF} = [V_{TH} + \eta V_T \ ln\ ln\ \left(\frac{I}{I_0\ S_2}\right)] + [\eta V_T \ ln\ ln\ \left(\frac{S_2}{S_3}\right)] + [\eta V_T \ ln\ ln\ (\frac{S_3}{S_4})]$$

$$V_{REF} = V_{TH} + \eta V_T \ ln\ ln\ \left(\frac{I}{I_0\ S_4}\right) \quad (16)$$

Now substitute the value of I from (7) and I_0 from (2) in (16)

$$V_{REF} = V_{TH} + \eta V_T \ ln\ ln\ \left(\frac{\frac{\eta V_T}{R_0} ln ln \left(\frac{S_{B1}}{S_{B0}}\right)}{\mu Cox\ (\eta - 1) V_T^2\ S_4}\right) \quad (17)$$

Upon simplifying, the output voltage reference turns out to be

$$V_{REF} = V_{TH} + \eta V_T \ ln\ ln\ \left(\frac{\eta ln ln \left(\frac{S_{B1}}{S_{B0}}\right)}{\mu Cox\ R_0 (\eta - 1) V_T\ S_4}\right) \quad (18)$$

This V_{REF} is then used to bias the gates of all PMOS current mirrors, which establishes the required stable current I for the given circuit. As illustrated in the above equation (18), the term V_{TH} represents the negative TC, and the term V_T symbolises a positive TC. Hence, it's apparent from (18) that the aspect ratios of transistor M_4, M_{B0} and M_{B1} have a positive impact on the temperature coefficient.

D. *Bias Current Generator*

The bias section could also be termed the second stage of the op-amp. It focuses on the active regulation of the reference current. As the transistors M_{B0} and M_{B1}, along with R_0 of the beta-multiplier, generate an error signal $V_N - V_P$, the op-amp then amplifies this error and produces DC output voltages which act as Control voltage at the gates of nearly every PMOS current mirror to set a precise and stable operating current throughout all branches. This bias current generator comprises two PMOS transistors, M_{C4} and M_{C6}, with their gates connected to V_{o1} and M_{C1}, with their gate and drain terminals shorted. Then the cascaded transistors M_{C5} and M_{C7} are connected to V_{o2}, and along with that, M_{C0} is connected in the same manner with its shorted gate-drain terminal and are cascoded to M_{C4}, M_{C6} and M_{C1}. The two NMOS transistors M_{C3} and M_{C2} are present with their source grounded and drain connected to M_{C4} and M_{C1}, respectively, and the drain and gate terminals of M_{C3} are shorted.

E. *Operational Amplifier*

The output of the operational amplifier serves as the bias for all current mirrors in the high PSRR voltage reference circuit. Where V_{o1} drives the gates of M_{B2}, M_{B3}, M_1, M_{C4} and M_{C6} and V_{o2} drives the gates of the cascode current mirrors (M_{B4}, M_{B5}, M_0, M_{C5} and M_{C7}). This feedback mechanism forces the differential current across R_0 to settle to the exact value needed for the CMOS Voltage reference; this guarantees a stable yet accurate reference current, i.e. I_{REF}, despite the fluctuations or variations in supply voltage or temperature. The Operational Amplifier in the given circuit is a Two-Stage Op-amp, which aims to enforce the balance condition of $V_P = V_N$ in the given circuit. The first stage comprises a Differential Amplifier, which senses the error voltage, and that is $V_N - V_P$ and is responsible for providing high gain. The two NMOS transistors M_{4p} and M_{5p} serve as the input pair, operating in the Subthreshold region. This input pair aims to sense the difference in the input voltages. Then there are two PMOS transistors, M_{2p} and M_{3p}, as the active load. M_{2p} and M_{3p} forms the current mirror load which converts the differential current output of M_{4p} & M_{5p} into a single-ended voltage signal. The additional two NMOS transistors M_{6p} and M_{7p} provide the constant bias current for the differential pair. Hence, the Op-amp operates in a quiescent balanced state, i.e. the tail current of these two transistors is near zero. The second stage of the op-amp then further amplifies the signal and aims to generate the required control voltages for the suggested reference circuit. The PMOS transistor M_{1p} serves as the load/gain element for the second stage by driving the V_{o1} node. It's the only device in strong inversion linear, hence

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suggesting that it behaves as a low impedance driver to rapidly set the control voltage. Another diode-connected PMOS transistor M_{8p} performs as a load for the V_{01} output voltage. Then, these two transistors are cascoded with M_{0p} and M_{9p} to drive the final control voltages V_{o1} and V_{o2}, which ensures a higher PSRR.

III. SIMULATION RESULTS AND DISCUSSION

Utilising 180 nm CMOS technology, simulations for the proposed CBCVR have been carried out using a 0.9 V supply voltage at room temperature. This design delivers a stable and well-regulated output.

A. Reference Voltage and Line Sensitivity

The Proposed CBCVR circuit operates from a wide supply range from 0.9 V to 3.0 V, as illustrated in the Fig 2, giving the precise output voltage of 430.23 mV and its magnified view is shown in the Fig 3. The line sensitivity quantifies the variation in the output voltage corresponding to the variations in the supply voltage; thus, the calculated value is 0.00085 %/V as shown in the Fig 3.

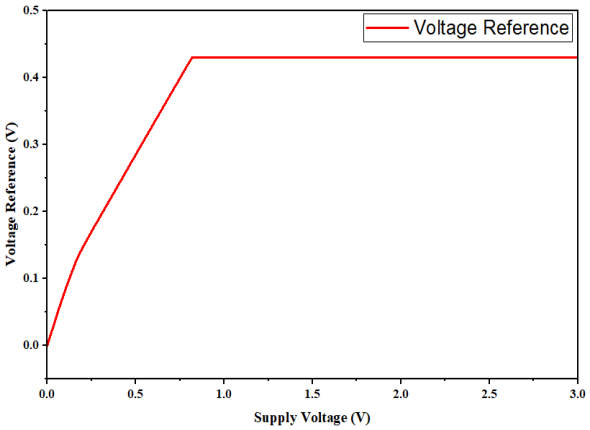

Fig. 2- Reference Voltage of the proposed CBCVR Circuit

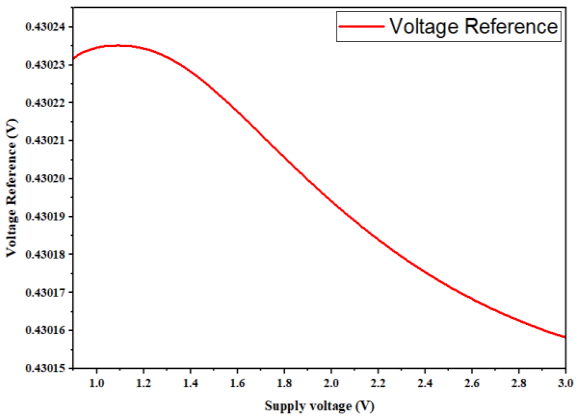

Fig. 3 Line sensitivity of the proposed CBCVR

B. Output Noise and Power Supply Rejection Ratio

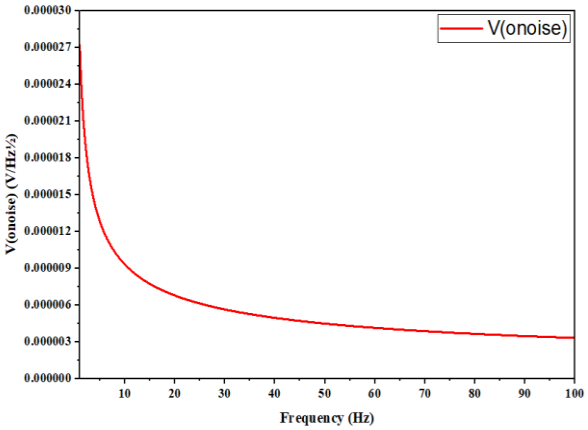

Fig. 4- Output Noise of the CBCVR

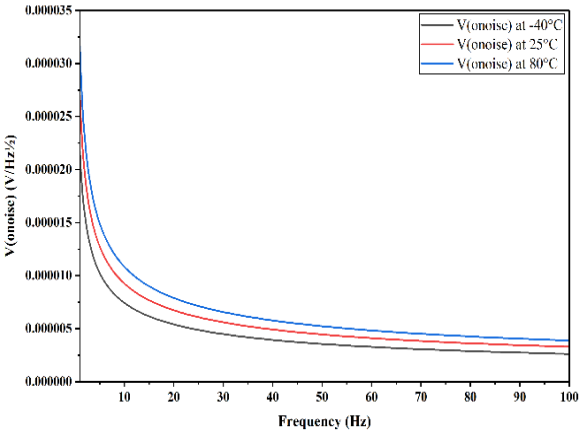

Fig. 5- Output Noise under Temperature Variation

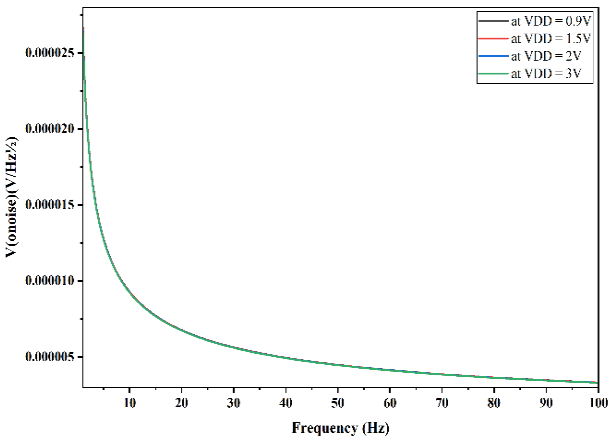

Fig. 6- Impact of different Supply Voltages on Output Noise

To access noise performance, the voltage noise spectral density was analyzed under three operating conditions: frequency variation, temperature dependence, and supply voltage fluctuation. Frequency Response of the output noise, as shown in Fig. 4, the reference exhibited a typical 1/f noise profile, with increased noise levels at low frequencies and a gradual decline as frequency increased. Exhibiting the total output noise to be 27.17 nV/√Hz, 9.31

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nV/√Hz and 3.31 nV/√Hz at 1Hz, 10Hz and 100Hz, respectively.

Output Noise under Temperature Variations, as shown in Fig. 5, was conducted at −40°C, 25°C, and 80°C. The noise magnitude increased subsequently with the increase in temperature, as seen in the Fig 5. At a frequency 1Hz, the measured output noise turns out to 21.54 nV/√Hz, 27.17 nV/√Hz and 31.63 nV/√Hz at -40°C, 25°C & 80°C, respectively. The impact of different Supply Voltages on Output Noise is illustrated in the Fig. 6. The output noise was evaluated at various supply level voltages, i.e. VDD of 0.9V, 1.5V, 2V, and 3V, which are of value 27.17 nV/√Hz, 27.03 nV/√Hz, 26.93 nV/√Hz and 26.83 nV/√Hz, respectively at a frequency of 1Hz. All curves demonstrated consistent noise behaviour across the frequency spectrum, with negligible deviation between supply voltages.

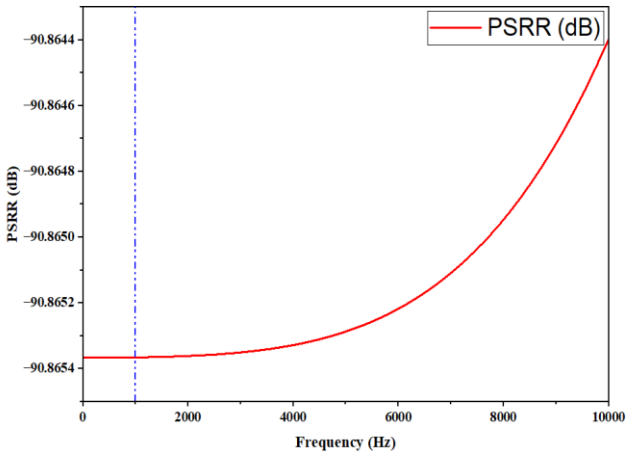

Fig. 7- PSRR

The PSRR of the CBCVR was evaluated across a frequency range of 1–10 kHz. As shown in Fig. 7, the PSRR remains consistently high throughout the spectrum, with a slight upward trend at higher frequencies. At 1 kHz, the circuit achieves a PSRR of −90.86 dB.

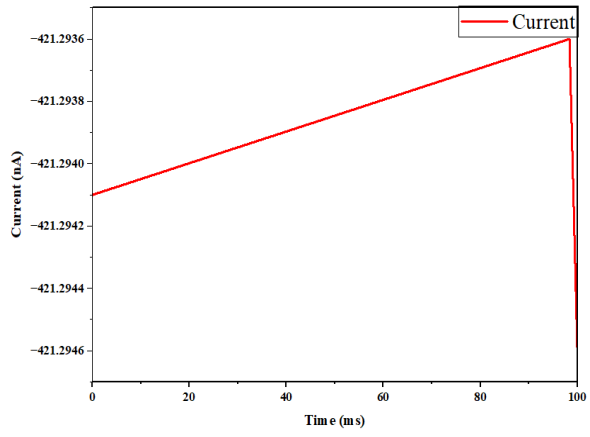

Fig. 8- Current drawn from the source

Under a nominal supply voltage of 0.9V, the CBCVR draws 421.29nA current from the source as shown in Fig.8.

C. Temperature Coefficient

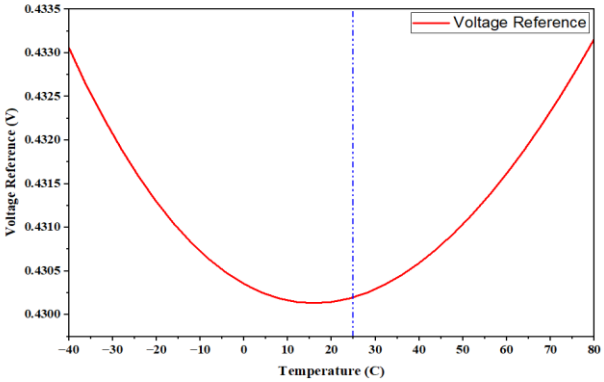

Fig. 9- Impact of Temperature on V_{REF}

The TC of the Proposed CBCVR was evaluated over a range of −40 °C till 80 °C. As depicted in Fig. 9, the observed output voltage exhibits a parabolic trend, reaching its minimum near room temperature (25 °C) and increasing symmetrically at both lower and higher temperatures. The measured TC was found to be 58.2 ppm/°C.

IV. CONCLUSIONS

The Proposed CBCVR shows an effective balance among the energy efficiency and the output accuracy, enabling its application for next-generation low-power systems. Through the use of cascode biasing and a dedicated amplifier stage, the design achieves good regulation against supply variations, evident in its PSRR of −90.86 dB and line sensitivity of just 0.0008 %/V. Despite its minimal power footprint of 379.16 nW, the circuit maintains consistent behaviour across temperature extremes, i.e. with a coefficient of 58.2 ppm/°C & low output noise that is of 27.17nV/√Hz. These results confirm the circuit's suitability for integration into mixed-signal platforms where power and accuracy are critical.

A comparative analysis of the suggested CBCVR's performance against other published voltage references is provided in Table 2. Table 2 illustrates that the proposed work achieves a remarkably low Line Sensitivity of 0.00085 %/V, which is significantly superior to the values reported in [5], [6], [13], [14], [15], [16], [17], [18]. Furthermore, the suggested design exhibits a PSRR of -90.86 dB at 1 kHz, outperforming all other compared references, which range from -35.77 dB to -84 dB. Notably, the proposed CBCVR demonstrates exceptional noise performance with an output noise of only 27.17 nV/√Hz at 1 Hz, which is several orders of magnitude lower than [5, 14]. While the voltage references cited in [6], [13], [14], [18] are also operational with supply voltages below 1V, the proposed design maintains an ultra-low power consumption of 379.16 nW across a broad supply range of 0.9 V to 3.0 V. Moreover, the proposed CBCVR demonstrates better power consumption than [5], [13], [14], [16], [17]. Future Work will focus on post layout validation and silicon fabrication. The primary scope of this paper is to

978-81-689089-0-1

introduce the architecture & validate its theoretical framework through simulation. Some analysis would require rigorous derivation, thus plan to present the Monte Carlo & Small signal analysis in our extended journal version of this work.

TABLE 2.
COMPARISON OF CURRENT STATE OF THE ART

Parameter	This work	[5]	[6]	[13]	[14]	[15]	[16]	[17]	[18]
Technology (nm)	180	180	90	90	180	180	180	180	180
Supply voltage (V)	0.9 to 3	1.8 to 3.5	0.8 to 1.32	0.5 to 3.3	0.9 to 3	1.2 to 1.8	1 to 2.5	3 to 5	0.9 – 2
Power(nW)	379.16	35,050	347	670	5,600	100	700	45,000	70
Line sensitivity (%/V)	0.00085	0.16	0.057	1.65	0.14	6.47	0.35	0.08	0.1
PSRR (dB)	-90.86 @ 1Hz to 1KHz	-42.1@ 100Hz	-84 @100Hz	-50 @10KHz	-35.77 @1KHz	-62 @100Hz	− 53.81@ 1 Hz to 10 kHz	− 76 @ 10Hz	-54@100Hz -37@10KHz -44@1MHz
Temperature range(°C)	-40 to 80	-40 to 85	-40 to 125	-40 to 130	-40 to 200	-40 to 120	− 40 to 140	− 55 to 125	-40 to 125
Mean TC (ppm/°C)	58.2	42.5	12.58	16.28	14.5	147	7.5	25	58.3
Output noise (nV/√Hz)	27.17 @1Hz 9.31 @10Hz 3.31 @100Hz	19,730 @0.1Hz	-	-	320 @100KHz 200 @1MHz	-	-	-	-

REFERENCES

[1] C. Nechifor, A. Dias, and L. Matei, "A novel low-power subthreshold voltage reference circuit with enhanced PSRR," in *Proc. 39th Conf. Des. Circuits Integr. Syst. (DCIS)*, Catania, Italy, 2024, pp. 1–6.

[2] H. Rashidian, I. Soltani, and M. Maghsoudi, "A 75.12-nW 0.5-V MOS-based BGR with curvature compensation for ADCs," *AEU - Int. J. Electron. Commun.*, vol. 191, p. 155678, 2025.

[3] F. Olivera and A. Petraglia, "Adjustable output CMOS voltage reference design," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 67, no. 10, pp. 1690–1694, Oct. 2020.

[4] H. Aminzadeh and M. M. Valinezhad, "0.7-V supply, 21-nW all-MOS voltage reference using a MOS-only current-driven reference core in digital CMOS," *Microelectron. J.*, vol. 102, p. 104841, 2020.

[5] S. Banerjee, S. Chatterjee, K. Mukherjee, and S. Pandit, "A temperature compensated beta-multiplier based sub-1 V voltage reference circuit for low-voltage applications," in *Proc. IEEE Dev. Integr. Circuit (DevIC)*, Kalyani, India, 2023, pp. 291–295.

[6] Q. Chen, J. Xie, H. Qiu, J. Li, and Z. Luo, "A high-performance CMOS voltage reference in one simple circuit," *AEU - Int. J. Electron. Commun.*, vol. 173, p. 155030, 2024.

[7] T. Cheng, H. Rao, and J. Wei, "An 8.83 ppm/°C temperature coefficient, 75 dB PSRR subthreshold CMOS voltage reference with piecewise curvature compensation," *Integration*, vol. 97, p. 102209, 2024.

[8] A. Wang, Y. Sun, and Z. Zhang, "A 15.4 nW, 59 ppm/°C CMOS voltage reference circuit with process and temperature compensation," *Microelectron. J.*, vol. 160, p. 106664, 2025.

[9] T. Cheng and X. Gong, "A 1 V supply 10.3 ppm/°C 59 nW subthreshold CMOS voltage reference," *Microelectron. J.*, vol. 152, p. 106389, 2024.

[10] L. Magnelli, F. Crupi, P. Corsonello, C. Pace, and G. Iannaccone, "A 2.6 nW, 0.45 V temperature-compensated subthreshold CMOS voltage reference," *IEEE J. Solid-State Circuits*, vol. 46, no. 2, pp. 465–474, Feb. 2011.

[11] M. Jiang, Y. Li, and Z. Yang, "A 3.9ppm/°C 8.8nW and high PSRR subthreshold CMOS multiple voltage reference," *Chinese J. Electron.*, vol. 26, no. 1, pp. 101–105, 2017.

[12] H. Yue *et al.*, "16.8/15.2 ppm/°C 81 nW high PSRR dual-output voltage reference for portable biomedical application," *Electronics*, vol. 8, no. 2, p. 213, 2019.

[13] H. Reddy and P. Arora, "A 16.28 ppm/°C temperature coefficient, 0.5 V low-voltage CMOS voltage reference with curvature compensation," *arXiv preprint arXiv:2508.15729*, 2025.

[14] K. Duggal, R. Pandey, and V. Niranjan, "A low temperature coefficient CMOS voltage reference for wide temperature range," in *Proc. 1st Int. Conf. Electron. Commun. Signal Process. (ICECSP)*, New Delhi, India, 2024, pp. 1–5.

[15] Y. Osaki, T. Hirose, N. Kuroki, and M. Numa, "1.2-V supply, 100-nW, 1.09-V bandgap and 0.7-V supply, 52.5-nW, 0.55-V subbandgap reference circuits for nanowatt CMOS LSIs," *IEEE J. Solid-State Circuits*, vol. 48, no. 6, pp. 1530–1538, June 2013.

978-81-689089-0-1

[16] K. Duggal, R. Pandey, and V. Niranjan, "A low-temperature coefficient, low power, and area-efficient temperature-compensated CMOS voltage reference for energy harvesting systems," *Analogue Integr. Circ. Sig. Process.*, vol. 124, no. 42, 2025.

[17] Y. Shi, S. Li, J. Cao, Z. Zhou, and W. Ling, "A 180 nm self-biased bandgap reference with high PSRR enhancement," *Nanoscale Res. Lett.*, vol. 15, no. 1, p. 104, 2020.

[18] L. Wang, C. Zhan, J. Tang, and G. Li, "An amplifier-offset-insensitive and high PSRR subthreshold CMOS voltage reference," *Int. J. Circ. Theor. Appl.*, vol. 46, no. 2, pp. 259–271, 2018.

Cite this article as:

Sarah, Vandana and et. al. "A Nano-Power Cascoded β-multiplier CMOS Voltage Reference with -90 dB PSRR 0.00085%/V Line Sensitivity", Proceedings of 13th international conference on Microelectronics, Circuits and Systems, Micro2026, (Vol-II).

Displayed as online on 14th July 2026.

Link: http://actsoft.org/science/micro2026-pro/116-micro2026.pdf

978-81-689089-0-1