

A Simulation Study of Gate-Pocket Overlap Dual Metal Hetero- junction Tunnel Field-Effect Transistor

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ABSTRACT

This study proposes a new configuration called Hetero-stacked Dual Metal Gate Tunnel Field-Effect Transistor (HS-DMG-TFET). The suggested device showcases enhanced ON-state current (I_{ON}), a heightened I_{ON}/I_{OFF} current ratio, and decreased sub-threshold swing, representing a substantial advancement in both DC and switching performance compared to existing TFET topologies. The proposed design includes a dual-metal gate featuring Molybdenum and Aluminium, which overlaps with the Si-Ge pocket. The resulting modifications in electron flow and tunneling behavior within the device lead to improvements in various performance metrics. Significantly, an I_{ON}/I_{OFF} ratio of $\sim 10^{14}$ is attained, with an ON-state current of 1.41×10^{-3} A/ μ m and an OFF-state current of 1.17×10^{-17} A/ μ m. The device also exhibits a significantly reduced sub-threshold slope, measuring 9.52 mV/dec, indicating superior transient performance. These DC characteristics underscore the potential of utilizing composite material gates for low-power applications, showcasing their advantages over traditional single-metal counterparts. Besides, enhanced transconductance and other RF performance metrics have been obtained for suggested device which confirms the device's suitability for a variety of analog and RF applications.

Keywords: Tunnel-Field-Effect-Transistor, Subthreshold Slope, Composite-Gate, Molybdenum, Low Power, High-Frequency Applications

1. INTRODUCTION

All microprocessors are designed using CMOS transistors. The microelectronics industry has been significantly influenced by MOSFET design in recent decades, as it boasts notable advantages such as minimal power dissipation, a broad range of supply voltages, noise tolerance, and high packaging capacity that contribute to improved efficiency [1]. The semiconductor industry minimizes device size, aiming for superior compactness or reduced die area, and enhanced functionality. However, aggressive scaling beyond a certain threshold negatively impacts system efficiency, diminishing its effectiveness in

RF and low-power applications [2]. Significantly, the effort to scale MOSFETs in alignment with Moore's law has encountered limitations termed as short channel effects [3]. At the same time, the significance of power management has increased, as technology scaling advances, leading to substantial short-channel effects (SCEs). Various SCEs, such as DIBL, threshold voltage roll-off, heightened I_{OFF} , deterioration in the I_{ON}/I_{OFF} (ON-current to OFF current ratio), and increased gate leakage current (I_g) [4]. Hence, there is a growing need to explore alternative technologies capable of surpassing the restrictions of CMOS technology, presenting a potential future solution and acting as a successor to traditional MOSFETs [5].

The Tunnel Field-Effect Transistor (TFET) was introduced as a superior alternative to the MOSFET, leveraging the advantages of quantum tunneling. Capitalizing on its Band-to-Band current conduction mechanism, TFET stands out as a promising device capable of achieving sub-60 mV/decade subthreshold swing (SS). The unique characteristics of TFET, including its Band-to-Band Tunnelling (BTBT) current conduction, contribute to mitigating Short-Channel Effects and achieving low OFF-state current (I_{OFF}). These features position TFET as an energy-efficient solution for use in low-power applications, making it a viable candidate for transitioning to a more power-efficient technology [6].

However, the drain current of TFET continues to pose a challenge, despite offering a favorable I_{ON}/I_{OFF} ratio, which supports its potential as a replacement for traditional MOSFETs. Certain engineering systems involving structural and material modifications have been successfully implemented [7]-[8], to concurrently enhance current, reduce leakage current, and achieve a steeper subthreshold slope. Utilizing the same materials in the source, channel, and drain regions leads to a diminished drain current in TFETs in contrast to MOSFETs. This is due to the dependence of electron tunneling from the source to the channel on the energy gap

between the valence band of the source and the conduction band of the channel.

The utilization of materials characterized by narrow energy band gaps, such as germanium (Ge) and silicon germanium (Si-Ge), is a deliberate approach to enhancing the performance of tunnel field-effect transistor structures. This deliberate material selection aims to narrow the energy band gap, resulting in a more pronounced exponential increase in the probability of band-to-band tunneling within the device [9]. The adoption of germanium in the source region is instrumental in reducing noise levels and enhancing the ON current [10]. To optimize the tunneling effect in TFETs, P-Pockets are employed. However, a significant challenge lies in the substantial tunneling resistance at the tunneling junction, which limits the ON-state current of TFET and thereby constrains its applicability in high-speed integrated circuits [11]. As per studies [12]-[13], employing dual metal gate (DMG) configurations, featuring distinct work function metals (with a tunneling gate positioned near the source and an auxiliary gate positioned near the drain), proves to be an efficient method for mitigating short-channel effects in TFET devices without introducing any negative impacts. By considering the advantages associated with DMG like, 2D-material, variable band gap, good carrier mobility, low OFF-state leakages, and compatibility with High-K dielectrics. Moreover, the fast-growing wireless communication sector drives demand for crucial RF and AMS technologies in the semiconductor industry [11]. Therefore, a comprehensive study on the RF characteristics of the proposed structures was conducted in this work. The investigation involved detailed analysis and simulations to assess performance. Various parameters were evaluated to ensure accuracy and reliability of the findings. The results provide valuable insights into the RF behaviour of this proposed structure.

The proposed HS-DMG-TFET has been evaluated against several recently introduced TFETs featuring distinct device topologies, as illustrated in Table I. The proposed device demonstrates an enhanced subthreshold slope (where a lower value is preferable) and I_{ON}/I_{OFF} ratio when compared to alternative devices in the study.

This study explores the effects of a hetero-stacked source, incorporating Si-Ge, a P-pocket design situated on the source side, and a dual material gate, on a range of device parameters. These parameters encompass drain current, sub-threshold swing, current switching ratio (I_{ON}/I_{OFF}), and transconductance.

TABLE I
COMPARISON OF CHARACTERISTICS BETWEEN
PROPOSED AND COMPARATIVE DEVICES.

Devices	SS (mV/dec)	I_{ON}/I_{OFF} ratio
TM-ES-DGV TFET [14]	43	10^{11}
ESDG-TFET [15]	12.24	10^{12}
CSP-DMUN-TFET [16]	13	10^{11}
Proposed Device	9.52	10^{14}

This paper presents hetero-stacked and DMG engineering aspects to improve the performance of the TFET. The paper is organized into five sections. Section I introduces previous works in the literature, Section II outlines the device topology. Section III details the simulation setup, including the employed models and methodologies, Section IV presents the results and initiates discussions, followed by Section V which concludes the paper and includes a compilation of the utilized references.

II. STRUCTURAL DESCRIPTION AND EXPOSITION

Fig. 1 illustrates the schematic depiction of the Hetero-stacked dual metal gate Tunnel field effect, accompanied by a custom design specifically designed for low-power applications. The primary objective of this innovative device is to ensure optimal functionality while minimizing power consumption, irrespective of its designated application. Table II comprises the comprehensive set of structural dimensions regarding the proposed device.

The HS DMG-TFET features a dual-layered source structure incorporating two distinct materials. The upper source layer utilizes silicon semiconductor material, while the underlying layer employs germanium, a semiconductor with a smaller bandgap compared to Si. To minimize leakage current, Si, with its larger bandgap, is employed in the channel and drain regions. The Ge layer in the source enhances band-to-band tunneling efficiency, leading to increased drain current with rising gate voltage [17]. This improvement in subthreshold characteristics results in a sharper average subthreshold swing. In the heterojunction setup, a P-layer pocket is introduced near the source-channel junction, leading to the bending of energy bands, and amplifying the ON current [18].

Molybdenum's high melting point, low coefficient of thermal expansion, and low electrical resistivity make it an ideal material for enduring the thermal demands in semiconductor manufacturing compared to doped polysilicon. In the proposed design, the simulation incorporates distinct device parameters, incorporating a high-k dielectric material featuring HfO₂ at a gate oxide

thickness of 2 nm. The gate comprises layers of aluminum and molybdenum positioned on top of the HfO₂ [19].

The device setup proposed includes a total length of 100 nm. Within this setup, the source, drain, and channel regions measure 20 nm, 27 nm, and 50 nm, respectively. Additionally, there's a p-pocket with a thickness of 3 nm, and the gate width (W_g) is 3 nm. The gate, comprising Aluminium and Molybdenum measures 27 nm and 25 nm, respectively, in the lateral direction.

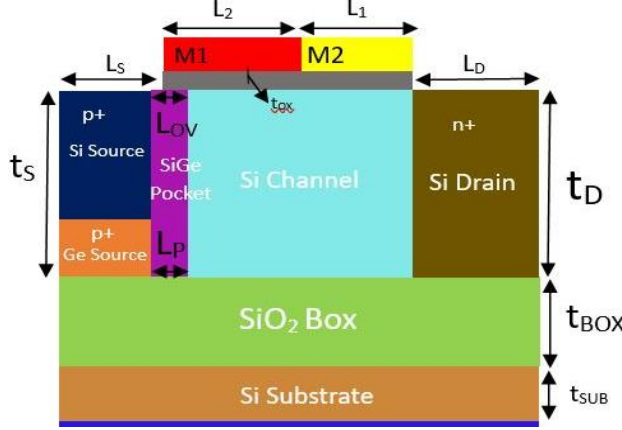


Fig. 1. Structure diagram of the proposed HS-DMG-TFET

The drain, source, pocket, and channel regions each have a thickness of 20 nm. A 10 nm thick SiO₂ box is used, followed by a substrate layer of 500 μm thick. The following represents the extrinsic doping profile: Source region is p-type which is heavily doped at $5 \times 10^{19} \text{ cm}^{-3}$, the drain is n-type moderately doped at $5 \times 10^{17} \text{ cm}^{-3}$, there is a p-pocket design doping at $1 \times 10^{18} \text{ cm}^{-3}$, the channel region which is p-type doped with a concentration of $1 \times 10^{16} \text{ cm}^{-3}$, and the substrate is p-type doped at $1 \times 10^{16} \text{ cm}^{-3}$.

TABLE II
OPTIMIZED DEVICE DIMENSIONS

Parameters	Symbols	Values
Source length (nm)	L_S	20
Drain length (nm)	L_D	27
Channel length (nm)	L_{Ch}	50
Pocket length (nm)	L_p	3
Substrate thickness (μm)	t_{SUB}	500
SiO ₂ Box thickness (nm)	t_{box}	10
Auxiliary gate (Mo) length (nm)	L_1	25
Tunneling gate (Al) length (nm)	L_2	27
Gate pocket overlap (nm)	L_{OV}	2
HfO ₂ thickness (nm)	T_{OX}	2
Source/Drain thickness(nm)	t_S/t_D	20
Source doping (cm^{-3})	N_A	5×10^{19}
Channel doping (cm^{-3})	N_{CH}	1×10^{16}
Drain doping (cm^{-3})	N_D	5×10^{17}
Pocket doping (cm^{-3})	N_A	1×10^{18}
Auxiliary gate work function (eV)	ϕ_{M2}	4.53
Tunneling gate work function (eV)	ϕ_{M1}	4.1

III. SIMULATION SETUP

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With the help of Sentaurus TCAD Tools Environment numerical simulation have been performed successfully [20]. Various models were utilized in the study, encompassing the OldSlotBoom model, the non-local BTBT model, the Shockley-Read-Hall (SRH) model, a doping-dependent model, and the Fermi model, as detailed in the below discussion. The discussion carries the special functioning details of the different TCAD models. The OldSlotBoom TCAD model has a band gap narrowing model. The Non-local BTBT model has Inter Band tunnelling. For considering the quantization of carrier density gradient the SRH TCAD model is used. To activate Fermi-Dirac statistics, Fermi A TCAD model is utilized, incorporating variations in doping concentration to accurately represent the impact on carrier mobility [21].

IV. RESULTS AND DISCUSSION

In this section, various electrical characteristics of the HS-DMG-TFET are highlighted, encompassing both input and output features. Achieving favourable outcomes required precise optimization of device dimensions, materials, work function, and doping concentrations. To validate the accuracy of the simulation setup, the simulation data for the proposed device was calibrated against experimental data [22], as depicted in Fig. 2. The strong correlation between the two data sets confirms the reliability of the selected models.

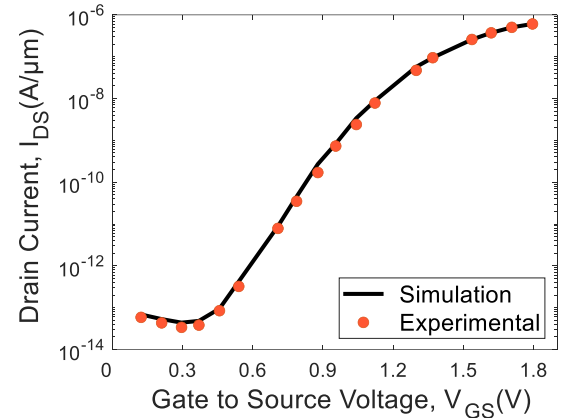


Fig.2. Calibration plot of the proposed TFET simulation and experimental data.

A. DC CHARACTERISTICS

The proposed design employs a composite gate consisting of two materials, namely Aluminium and Molybdenum, instead of a single material. These materials have distinct work functions, with M1 having a work function of 4.0 eV and M2 having a work function of 4.53 eV. M1 functions as the tunnelling gate and is composed of Aluminium, while M2 serves as the auxiliary gate and is composed of Molybdenum. Significantly, M1, positioned

on the source side, features a lower work function, whereas M2, situated on the drain side, possesses a higher work function. This specific configuration enhances the I_{ON}/I_{OFF} ratio compared to using a gate made of a single material [23].

The increase in I_{ON} can be attributed to the lower work function of tunneling gate material (Al) and overlap on the pocket region. The decrease in I_{OFF} can be attributed to the higher work function of the auxiliary gate material (Mo). Conversely, during the OFF state, the higher work function results in a reduction in overlap [24]-[25]. Conversely, the overlapping of the gate-pocket on the source side leads to higher band-to-band generation rate, as illustrated in Fig. 3(a), while Fig. 3(b) depicts variation of electron density throughout the proposed structure. Upon the application of gate voltage, it aligns the conduction band edge and valence band edge, causing them to approach each other closely, leading to the phenomenon of tunnelling, as illustrated in Fig. 3(c). The probability of tunneling is influenced by factors such as the height, width, and shape of the potential barrier, along with the mass of the charge carriers involved in the process. The rate of BTB tunnelling can be calculated using the Wentzel-Kramers-Brillouin (WKB) technique, as shown in equation (1) [7],[26].

$$T(E) \approx \exp\left(\frac{-4\lambda\sqrt{2m^*}E_g^{3/2}}{3|e|\hbar(E_g+\Delta\phi)}\right)\Delta\phi \quad (1)$$

where m^* is the reduced effective mass, E_g is the energy band gap, $\hbar$ is the reduced Plank's constant, $\Delta\phi$ = energy range within which tunneling occurs, λ = tunneling length, e = electronic charge, and t_{si} / t_{ox} = silicon film / dielectric constant thickness.

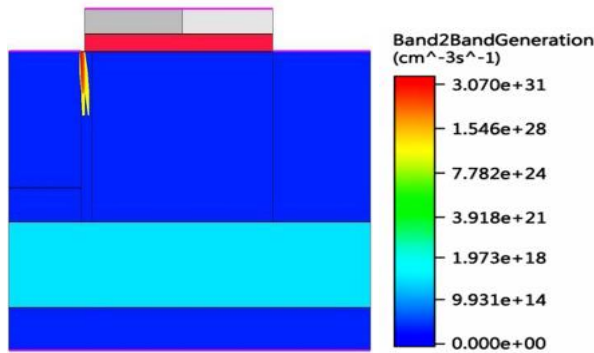


Fig. 3(a). Band to Band generation for proposed TFET.

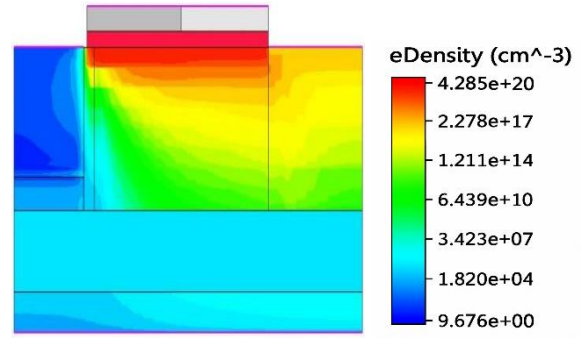


Fig. 3(b). Variation of eDensity throughout the proposed TFET.

Additionally, Fig. 3(d) depicts the electric field graphs plotted with respect to lateral distance along the device length for the HS-DMG-TFET. Notably, the maximum electric field value observed for HS-DMG-TFET is 8.2 V/cm. The heightened electric field in the HS-DMG-TFET is primarily due to the proximity of a high-k dielectric near the source region, resulting in an elevated field at the junction of the source and channel. This enhancement in the band-to-band tunneling rate, consequent to the elevated field, contributes to a higher ON-state current [27].

The transfer characteristics of the proposed TFET were examined by adjusting the gate-source voltage V_{GS} within the -0.2 V to 1.5 V range. The results obtained at three different V_{DS} values, 0.5 V, 0.7 V, and 0.9 V, are shown in Fig. 4(a) where the drain current is presumed to be represented in the equation (2) [28].

$$I_{ds} = I_0 e^{\left(\frac{(V_{gs}-V_t)}{\eta} \times V_t\right)} \quad (2)$$

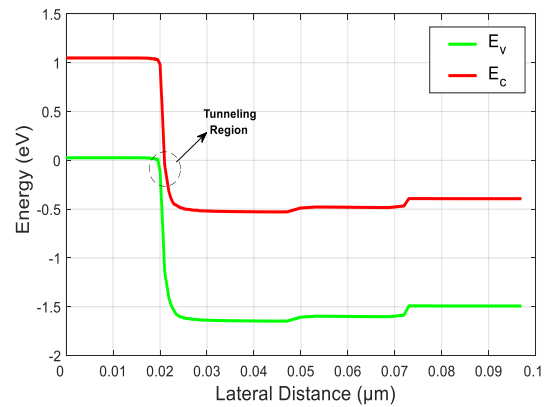


Fig. 3(c). Energy band diagram for proposed TFET

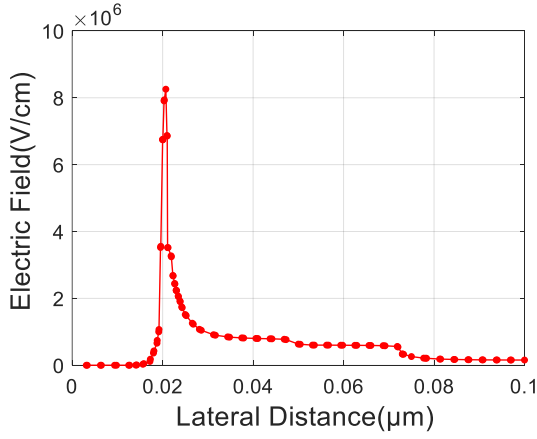


Fig. 3(d). Plot of electric field with respect to device length of HS-DMG -TFET at $V_{DS} = 0.5$ V

where I_0 stands for the subthreshold current, V_t denotes the threshold voltage, n represents the subthreshold slope factor, and the term 'exp' denotes the exponential function. Assuming that V_t is the threshold voltage, n is the subthreshold slope factor, and 'exp' is the exponential function, we get I_0 as the sub-threshold current. The results show that the dual metal TFET performs as expected, with a subthreshold swing (SS) of 9.52 mV/dec at $V_{DS} = 0.9$ V, a high on-current (I_{ON}) of 1.41×10^{-3} A/ μ m, and a minimal leakage current (I_{OFF}) of 1.17×10^{-17} A/ μ m, as shown in Table III.

TABLE III
DC CHARACTERISTICS OF PROPOSED OPTIMIZED STRUCTURE

Parameters	Value	Unit
I_{ON}	1.41×10^{-3}	A/ μ m
I_{OFF}	1.17×10^{-17}	A/ μ m
SS	9.52	mV/decade
I_{ON}/I_{OFF} ratio	1.21×10^{14}	Dimensionless

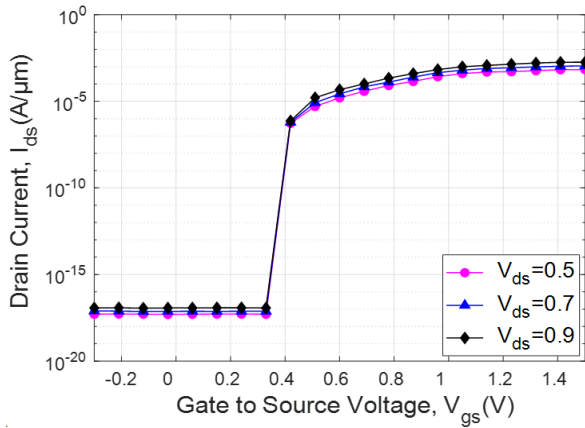


Fig. 4(a). Transfer characteristics of the proposed structure

The output characteristics for V_{GS} values at 0.5 V, 0.7 V, and 0.9 V are shown in Fig. 4(b). The impact of BTBT becomes increasingly evident when V_{GS} equals 0.9 volts, which raises the drain current. The on-current reaches saturation as the tunnelling rate reaches its maximum.

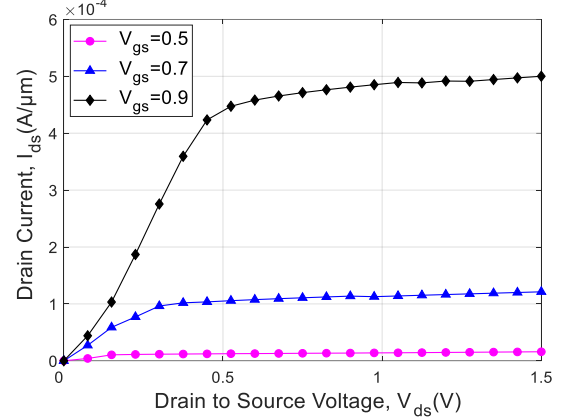


Fig. 4(b). Output characteristics of the proposed structure.

B. ANALOG/RF PARAMETERS

This section examines several key analog/RF performance parameters that are crucial in determining device performance. These parameters include total capacitance (C_{gg}), transconductance (g_m), output transconductance (g_{ds}) and cutoff frequency (f_T).

The parameters mentioned above are determined by applying a 1 MHz frequency signal to the input port.

Transconductance (g_m) is vital for attaining a higher cutoff frequency. The attribute g_m represents the change in drain current (I_{DS}) in response to a change in gate-source voltage (V_{GS}) while keeping the drain-source voltage (V_{DS}) constant, as defined by equation 3 [29].

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \quad (3)$$

The g_m attribute is crucial for determining device gain and designing analogue circuits. To ensure optimal high-frequency performance, the g_m bias point must be sufficiently large. Fig. 5 illustrates the transconductance of the proposed TFET. The plot shows that as V_{GS} increases, g_m rises until it reaches a maximum, then begins to decrease with further increases in V_{GS} . This decline in g_m is due to mobility degradation with rising V_{GS} . The graph indicates that the proposed TFET achieves a high g_m value of around 1.9×10^{-4} S. Therefore, the suggested TFET is suitable for high-frequency analog applications.

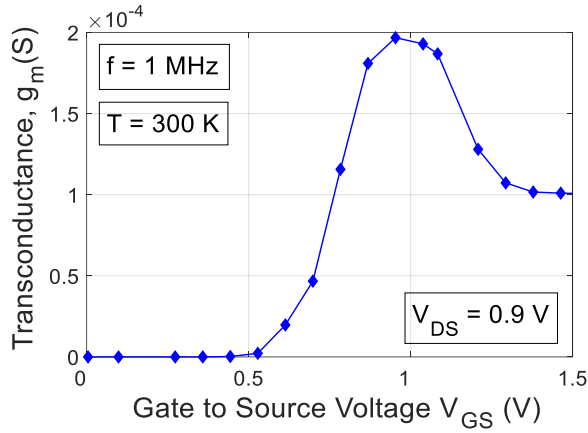


Fig. 5. Variation in transconductance with respect to V_{GS}

Moreover, output transconductance (g_{ds}) is the inverse of the device's output resistance. It represents how the drain current varies with the drain-source voltage and is described by equation 4. Fig. 6 highlights the significance of changes in output conductance with respect to V_{DS} at $V_{GS} = 0.9$ V.

$$g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} \quad (4)$$

Additionally, for optimal RF performance, a low C_{gg} value is desirable. Fig. 7 provides details on the overall gate capacitance (C_{gg}) of the proposed TFET framework in relation to the gate voltage. The figure shows that the (C_{gg}) value decreases at higher gate voltage. Moreover, the cutoff frequency (f_T) of the devices is directly related to g_m and inversely related to the total parasitic capacitance ($C_{gg} = C_{gs} + C_{gd}$), The expression for f_T is provided in equation 5 [25][29].

$$f_T = \frac{g_m}{2\pi(C_{gg})} \quad (5)$$

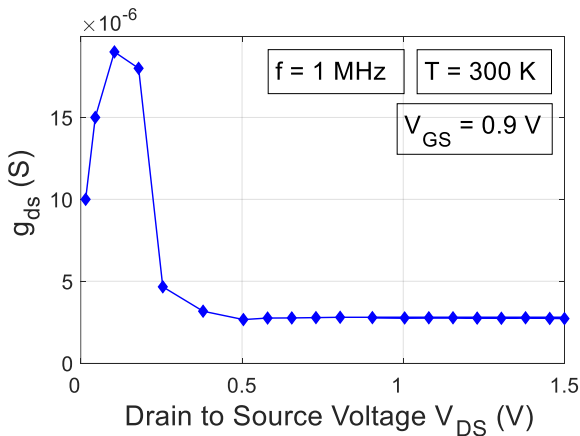


Fig.6 Variation in Output Transconductance with respect to V_{DS}

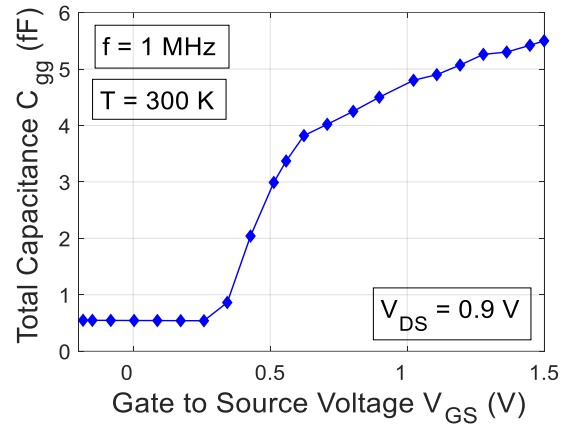


Fig. 7. Characteristics of the Total Gate Capacitance

Fig. 8 shows the f_T characteristics for the suggested TFET. The plot indicates that f_T increases with V_{GS} due to the corresponding rise in g_m . The plot shows that f_T increases with V_{GS} , which is due to the rise in g_m with increasing V_{GS} . However, f_T begins to decrease with further increases in V_{GS} , which is attributed to the combined effects of gate-source capacitance (C_{gs}) and gate-drain capacitance (C_{gd}), as well as a reduction in g_m due to mobility degradation. The plot demonstrates that the proposed TFET achieves a f_T of approximately 86 GHz, which is higher than that of traditional silicon based TFETs. Therefore, the proposed TFET is suitable for high-frequency applications.

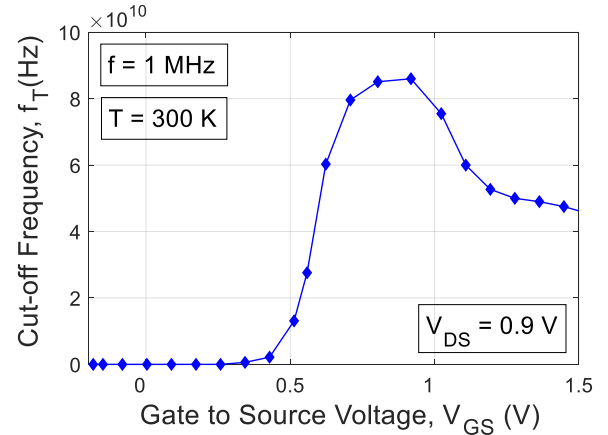


Fig.8. Variation in cutoff frequency with respect to V_{GS}

V. CONCLUSION

This paper explores the DC characteristics of a suggested hetero-stacked TFET structure featuring dual gate metals of molybdenum and aluminium, along with a Si/Ge pocket. The simulations of the presented TFETs are carried out using Sentaurus TCAD tool. When Aluminium and Molybdenum are employed as a dual gate composite material, there is an observed enhancement in the I_{ON}/I_{OFF} ratio and a remarkable improvement in SS . The structure showcases outstanding performance in solid-state

applications, making it appropriate for high-speed switching devices. Moreover, its increased I_{ON} current capacity facilitates a larger fan-out, enabling the control of more devices. On the flip side, the decreased I_{OFF} similarly plays a role in diminishing power usage when the system is inactive. In RF analysis, the FOM parameter exhibits a higher value compared to conventional TFETs, indicating that the suggested TFET may be more suitable for high-frequency applications. Based on the comprehensive RF and DC performance analysis, it is concluded that our suggested TFET (HS-DMG-TFET) is a superior candidate for low-power and high-frequency applications.

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