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Design and Parameter Optimization of CMOS Operational Transconductance Amplifier (OTA)

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ABSTRACT

One of the essential components of an analog implementation using an OP-amp is an OTA. This work looks into the behavior and properties of OTA. The OTA circuit utilizes the design methodology that considers analog circuit sizing and automatic selection of analog components. Researchers in the OTA design due to its low supply voltage, linearity, and low power dissipation. The design of OTA has been widely studied and utilised in research and industry since the early days of integrated circuits. In this review, various techniques and approaches have been presented for the design of these components. The integration of massive numbers of components has made it challenging to create ideal analog circuits. An analog integrated circuit using the CMOS technology could be created by using an evolutionary approach to size a device. This review focuses on the various operations of the OTA circuits.

Keywords: Analog circuits, CMOS, OTA.

I. INTRODUCTION

The main building blocks of mixed-signal and analog electronic circuits are operational transconductance amplifiers. Experts believed that the end of analog circuits was approaching during the twentieth century due to the increasing reliance on digital signals. Even though the world is becoming more dependent on digital signals, most of them still require the use of analog circuits to process information. The design concepts of analog circuits are necessary for high-speed digital circuits. The design concepts of analog circuits are significant. Traditional methods can be time-consuming, difficult, and challenging to carry out. With the help of Optimization algorithms, it is now possible to eliminate the mystery of designing an analog integrated circuit [1].
Most integrated circuit systems are created in the digital domain, while analog functions are essential in various applications. The input signals of an electronic device are generally analog, they have to be filtered and amplified for digital conversion. [2]. The first systematic design automation techniques for finding procedures for the design of analog components were introduced [3].

In the concept of a knowledge-based design approach, a designer can translate ideas into a synthesis rule that can be used to represent a device's circuit specifications. The advantages of this approach are its fast execution time and its ability to update its design plan frequently. However, the time-consuming process of developing the design plan can be very challenging. The knowledge-based design approach was generally considered to be successful. However, it was not able to achieve a high accuracy due to the reduction of the analytical models [4].

At the current VLSI technology evolutionary stage, millions of millions transistors are stacked on a single chip. The evolution of mixed-signal analysis can be attributed to the digital and analog functions found in integrated circuits. The most important foundation for implementing mixed-signal systems is the CMOS technology. An operational amplifier is a vital design component for any analog system. The optimization of an analog IC, like OTA, is regarded as one of the most demanding and fascinating job in the analog IC design world [5].

The OTA is commonly used in many applications, like sensors, filters, ADC, compact devices, & bio-medical signal amplification [6]. An OTA has been regarded as a significant building block for various types of electronic devices, such as reconfigurable analog VLSI and signal processors. OTA offers a unique remarkable feature known as reconfigure ability that is commonly used in filter design. High-frequency filters require an excellent control ability and high trans-conductance. An OTA should also have better linearity to operate at a constant and stable frequency. This is why the design process of an

OTA should focus on providing adequate control ability [7].

To enhance the output efficiency of an OTA, some algorithms have been developed using bio-inspired heuristics to efficiently navigate through complex design spaces. These include the Genetic Algorithms (GA) [8], Simulated Annealing (SA) [9], Gravitational Search Algorithms (GSA) [10], Particle Swarm Optimization (PSO) [11], Ant Colony Optimization (ACO) [12], Firefly Algorithm (FA) [13], Cuckoo Search (CS) [14] Colliding Bodies Optimization (CBO) [15], and SOS (Symbiotic Organisms Search) Algorithms or a hybrid form of them. These algorithms have shown notable improvements in their performance metrics, like power consumption reduction and area reduction. PSO demonstrated exceptional convergence and effectiveness, achieving notable gate area and power consumption reductions. Outperforming other techniques, the Cuckoo Search algorithm was able to reduce power consumption by over 62% and achieve a remarkable gate area reduction of 31%. This demonstrates its exceptional ability to implement circuit optimization techniques [16]. The Firefly Algorithm was able to provide competitive results when it came to optimizing the gain and slew rate of operational amplifiers [17]. Firefly Algorithm is the first time it has been performed to optimize LNA parameters. It is mainly focused on minimizing NF and maximizing gains [18]. Firefly algorithm is highly multi objective optimizer, which is able to achieve the optimization of the various parameters of LNA such as input and output matching, linearity, Gain, and Noise Figure [19]. When integrated with the design methodology of gm/ID, the SOS algorithm was able to reduce the computational time and minimize input-referred noise [20].

The remaining sections are organized into these categories. The II section of the paper provides an overview of the OTA. We discuss the topologies of the OTA in section III. In section IV, we talk about the design methodology for the OTA. We highlight the transient response of the OTA in section V. In section VI, we discuss the automated sizing technique and its flow diagram in section VII. Section VIII of the paper reviews the performance improvement techniques of the current literature on two-stage operational transconductance amplifiers. Finally, in section IX, the conclusion has been presented.

II. OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

An OTA, is a type of electronic device in which a differential input voltage produces an output current. So, OTA is a VCCS (voltage control current source) device. An extra input for current control is typically used in an OTA to operate the device, which makes it similar to the conventional operational amplifier. This type of device features a high-impedance differential input stage that can be utilized with a negative feedback feature. The technological advancements that have occurred in VLSI technology have led to the minimization of the power supply and the size of CMOS. As a result, the OTA has become a vital building block for various analog integrated circuits, like instrumentation and neural networks. An OTA is similar to a conventional Op-amp in that both have differential inputs. The fundamental difference between them is that in the former, the output is current, while in the latter, it is voltage. An OTA is commonly used in the design of voltage-controlled filters (VCF) and voltage-controlled oscillators (VCO) for use in various electronic devices. An OTA primarily operates low-impedance sinks, like coaxial cables at high bandwidth. Traditionally, an OTA is implemented in a two-stage cascade to provide high gain. To scale CMOS technology's dimensions, the supply voltage must be proportional. Lower supply voltages lead to lower power consumption [21].

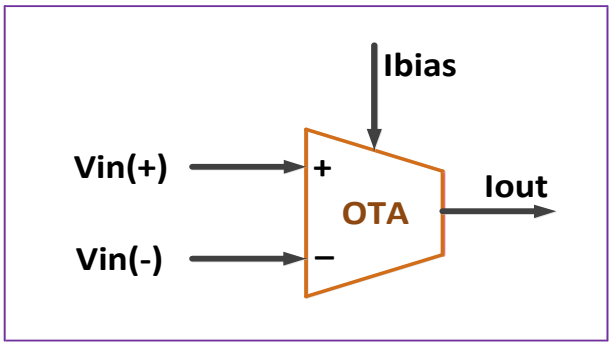

Fig. 1. Symbol of the OTA [22].

Fig 1 shows the symbol of the OTA. Trans-conductance refers to the process involved in converting an input voltage into an output current. It has two non-inverting (+Vin) and inverting (-Vin) input voltage terminals. The gain of the device is controlled by the Ibias current, which is relative to the trans conductance of OTA.

Fig 2 reveals the block diagram of two-stage OTA. It explains the second stage of an OTA, which involves the device's input. The subsequent stage can boost the yield voltage swing and improve the DC gain. Bias circuitry helps set the operating point of the individual transistor. Compensating circuitry is also utilized for stability [23].

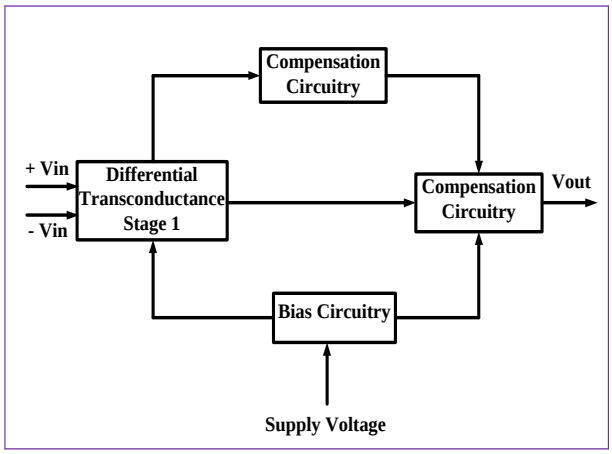

Fig. 2. Block diagram of two-stage OTA [24].

III. OTA TOPOLOGIES

Depending on its operation, an OTA may be classified as four different types.

A. Single-stage (Five Transistors) OTA

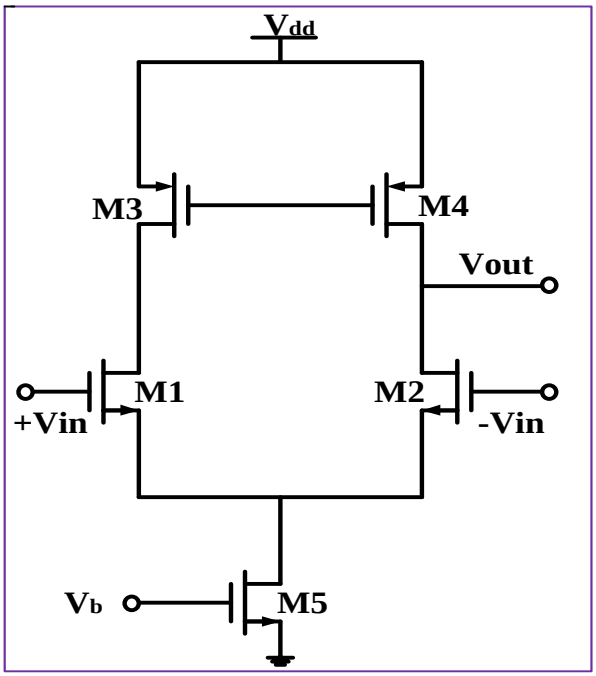

Fig. 3. Single-stage (Five Transistor) OTA [25].

The single-stage OTA circuit shown in Fig 3 consists of five transistors. A differential input pair is utilized for M1 transistor and M2 transistor as well as a current mirror source of M3 transistor and M4 transistor. The biasing activity of the device is carried out by using the MOSFET M5. The advantages of this single-stage OTA include its power consumption low, fast response, and very simple design. The disadvantage of this type of architecture is its low gain due to low output impedance.

B. Two-stage OTA

Fig 4 shows the two-stage OTA design. In a two-stage OTA design, M1, and M2 MOSFETs form a differential input pair, and M3, and M4 MOSFETs form a current mirror. The second stage, which is used for improving the gain, is composed of M6 and M7. The biasing activity is carried out by using M5 and M8. The coupling capacitor known as Cc can also be utilized to couple the two-stage design circuits.

An operational amplifier can be optimized using a weighted approach, which takes into account adaptive weights. The level of fitness of individuals can then be determined by taking adaptive weights into account in the optimization process. Net fitness of individuals

$$F = \sum_{i=1}^{n} \omega_i . f_i \qquad (1)$$

Performances are measured by weight coefficient ωi of a given sub-objective fi is determined by comparing its numbers i with the number of performances [26].

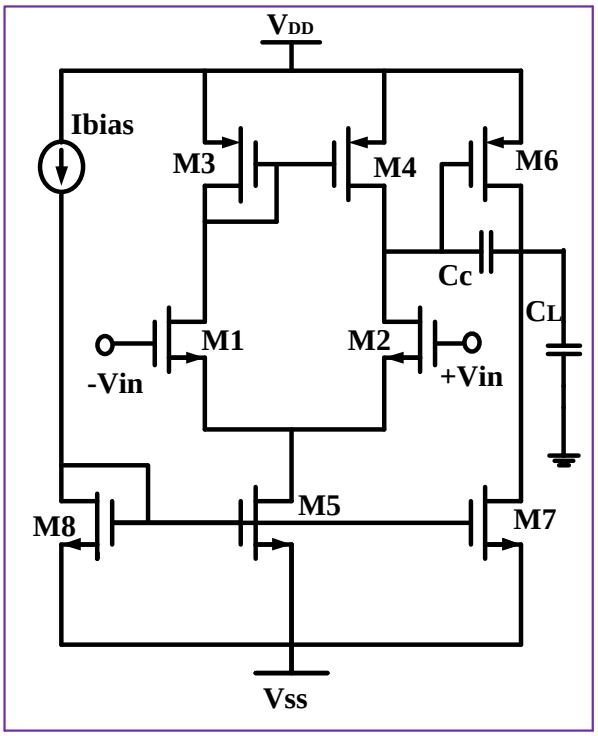

Fig. 4. Two-stage OTA [26] [27].

The design of a mixed-signal IC has a significant amount of effort involved in the sizing of its analog component. The design space for an IC is usually large due to the complexity of the component's size. This is why it's important to consider the optimization of the IC design. The performance evaluation of the three algorithms: the PSO, the Cuckoo Search (CS), and the FA, by comparing their sizes for a two-stage operation of the transconductance amplifier [27]. The advantage of this architecture offers higher gain than single-stage OTA and consumes less power than single-stage OTA. It also offers high unity gain. The disadvantage of this approach is its slow response. An additional stage can increase the complexity of the architecture and cause it to cost more [28].

Compensation Capacitor (Cc)

The simplest approach to optimizing the design of an electronic component is by implementing the Miller effect. This method involves connecting the various high-gain stages.

$$C_C \geq 0.22\, C_L \qquad (2)$$

Where C_L represents the load capacitor.

Differential Gain Stage (M1 & M2)

The M1 and M2 n- channel MOSFETs are utilized in the differential gain stage. They determine the UGB requirement and the gain of first stage.

Common Source Stage (M6)

The M6 p-channel MOSFET's transconductance can be determined by the current flowing in the second stage.

Current Mirror (M3 & M4)

The M3, M4, and M6 p-channel MOSFETs provide the load structure of the two-stage OTA circuit. The gm/Id value of the three transistors must be identical for matching to prevent offset at the output of the first stage.

Biased-Current Sink (M5 & M7)

The M5 transistor utilizes the differential pair to sink the current. The small size of this device is constrained by the minimum common-mode input voltage, CMRR, and, PSRR requirements.

C. Telescopic Cascode OTA

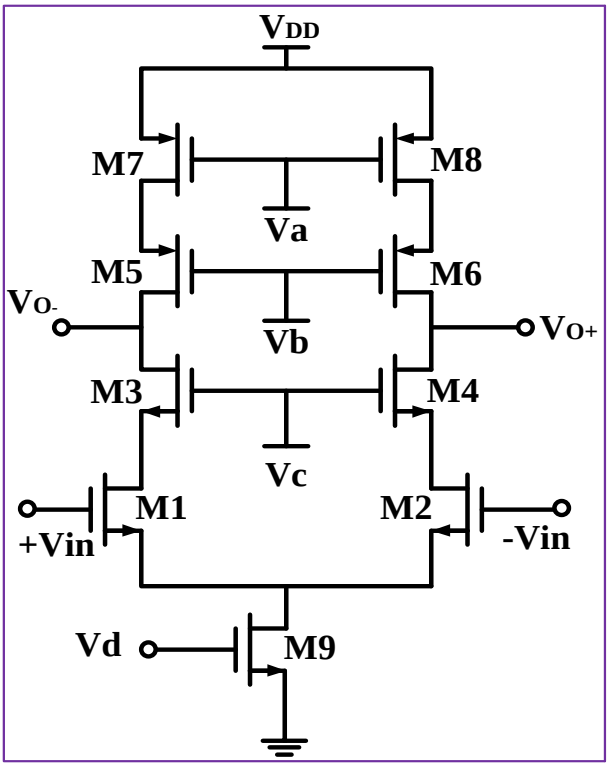

Fig. 5. Telescopic Cascode OTA [29].

Fig 5 shows the Telescopic Cascode OTA. The low gain caused by the single-stage OTA is mainly attributed to its low output impedance. To improve the gain, some additional MOSFETs are added at the output. The placement of the MOSFETs on one another can help improve their overall gain. This type of configuration is referred to as the cascode. The low power consumption and fast switching speed of the Telescopic Cascode OTA design are some of the advantages that make it an ideal choice for various applications. The drawback of Telescopic Cascode OTA design is its moderate output swing.

D. Folded Cascode OTA

Fig 6 shows the architecture of Folded Cascode CMOS OTA. Four of the MOSFETs are located on the output side of the device in the first stage. There is also a pair of differential input terminals. The second stage utilizes the first in a cascade to achieve high gain. The fast switching speed and moderate power consumption of the Folded Cascode OTA are some of its advantages. The ability to achieve high gain with high output impedance is a plus for this type of architecture. It contributes to high swing, high bandwidth, and high gain. The additional two legs of the Folded Cascodes OTA design consumes more power.

It also adds thermal noise to the signal due to complex circuits [29].

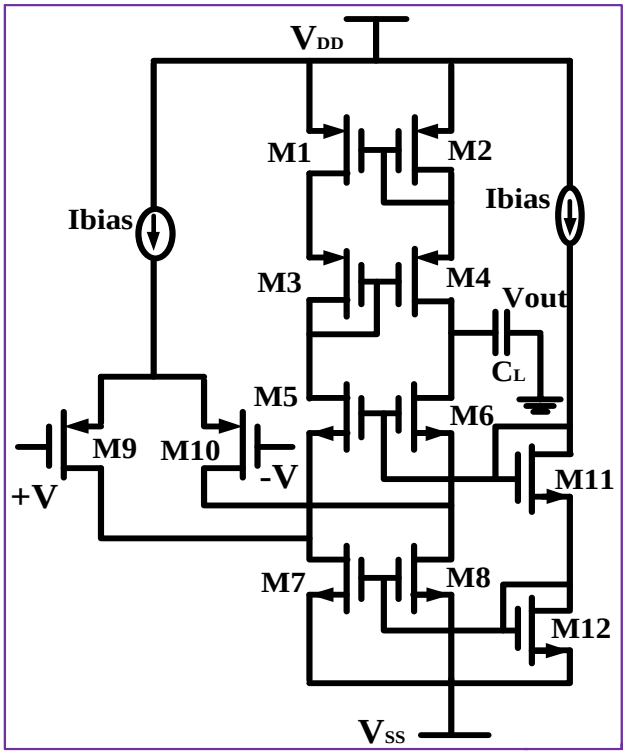

Fig. 6. The Architecture of Folded Cascode CMOS OTA [30].

The high slew rate, DC gain, and unity-gain frequencies of the CMOS Folded OTA are some of the characteristics that make it an ideal choice for various applications. The width, length, and bias current magnitude of the transistor, as well as the value of the resistors and capacitors, are some of the design factors that influence electronic device design [31].

DC open loop voltage gain

$$A_v = \frac{g_{M1}}{g_{ds2} + g_{ds4}} \times \frac{g_{M6}}{g_{ds6} + g_{ds7}} \qquad (3)$$

In eq (2), $gM1$ and $gM6$ are the trans-conductance of M1 and M6 transistors, and $gds2$, $gds4$, $gds6$, $gds7$ are the output trans-conductance of M2, M4, M6, and M7 transistors respectively [32].

Unity Gain Band Width

The UGBW of the two-stage OTA is determined by the expression given below [33].

$$\text{UGBW} = \frac{g_{M1}}{C_C} \qquad (4)$$

Slew rate

$$SR = \frac{I_5}{C_C} \qquad (5)$$

In eq (5), I5 and Cc are the current flows through transistor M_5 and compensation capacitance respectively [33].

Phase margin

$$PM = \pm 180 - Tan^{-1}\left(\frac{GBW}{P1}\right) - Tan^{-1}\left(\frac{GBW}{P2}\right) - Tan^{-1}\left(\frac{GBW}{z}\right) \qquad (6)$$

The total number of phase- shifts that occur at unity gain bandwidth (GWB) due to the zeros (z) and poles (p1 and p2) determines an operational amplifier's phase margin [34].

Power consumption

$$P = (V_{DD} - V_{SS}) \times (I_5 + 2I_7) \qquad (7)$$

In equation (7), V_{DD} and V_{SS} are the power supply. I_5 and I_7 are the current flows through MOSFET M_5 and M_7 respectively [35].

Operational Amplifier's area

$$Area = \sum_{i=1}^{k} W_i \cdot L_i \qquad (8)$$

In eq (8), Li and Wi refer to the lengths and widths of MOSFET gate transistors [34].

Common Mode Rejection Ratio

It is defined as the ratio of the differential mode gain (Ad) to the common mode gain (Ac).

$$CMRR = \left[\frac{A_d}{A_c}\right] \qquad (9)$$

TABLE I COMPARISON OF DIFFERENT OTA TOPOLOGIES [36].

Specifications	OTA Topologies			
	Single stage	Two-stage	Telescopic Cascode	Folded Cascode
Speed	Fast	Slow	Fastest	Fast
Gain	Low	High	Moderate	Moderate
Output Swing	Low	Highest	Moderate	Moderate
Power Consumption	Low	Moderate	Low	Moderate

An operational transconductance is a vital component of numerous analog circuits. It is also commonly utilized in time-sensitive systems and applications, such as oscillators, Gm-C filter systems, and wireless receiver networks. In numerous applications, the use of OTAs has been proposed as an alternative to conventional Op-Amps due to its ability to adjust bias current and high speed. For the first time, Nauta has proposed a differential trans-conductor that utilizes six CMOS inverters [37]. It is a powerful building block for developing high-frequency filters using an OTA. Since then, the use of CMOS inverters has also been widely used in developing circuits with an OTA [38][39].

IV. OTA DESIGN METHODOLOGY

The function of the OTA depends on the three design topologies shown in figure 7 below.

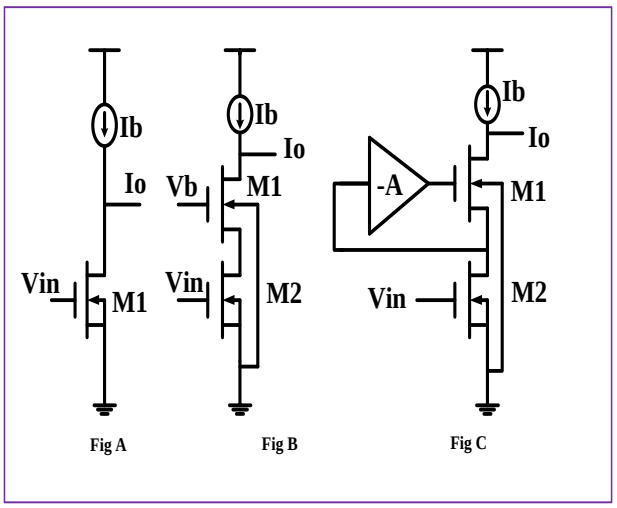

Fig. 7. OTA Design Methodology (A) Basic transconductance amplifier (B) Cascode transconductance amplifier (C) Regulated cascode feedback transconductance amplifier [22].

The basic transconductance amplifier shown in Fig 7A utilizes the saturation region to convert the input voltage into an output current. It also has a few limitations, such as low output impedance and linearity. The second topology of the OTA is referred to as a cascode trans conductance amplifier which is shown in Fig 7B. It utilizes the M1 MOSFET in the ohmic region and the MOSFET M2 in the isolation between both input terminal and output terminal. This makes the output impedance and linearity properties better. The third topology of the OTA is a regulated cascode feedback transconductance amplifier, shown in Fig 7C. It provides negative feedback with gain A, which amplifies the input voltage and enhances its linearity. Compared to other topologies, this topology provides better stability[40][41].

V. OTA TRANSIENT RESPONSE

The settling time of the OTA plays a vital role in the design and development of electronic systems. In order to enhance the system's transient response, different theoretical analyses and circuit modifications have been carried out [42]. The operation of the switching capacitor commonly utilizes an OTA circuit, and its transient response is divided into dead time, slewing, and settling which is shown in the below fig (8).

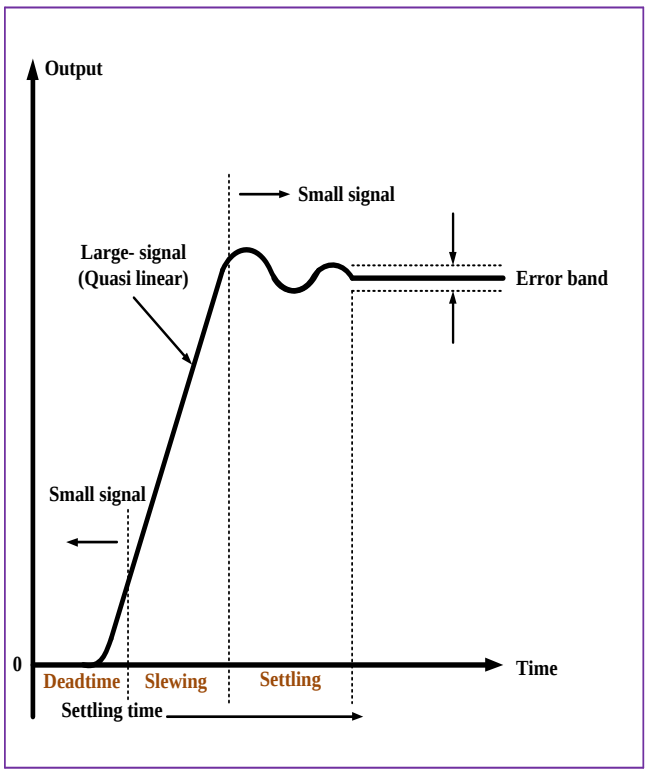

Fig. 8. OTA transient response [43].

The dead-time and the settling of an OTA are computed by taking into account the UGB and the small-signal speed. The output of the OTA should also be within the specified error range with the help of the transient response's settling time. The slew rate and unity-gain bandwidth of the OTA are proportional to the bias current (Ibias) and the square root of the bias current $(Ibias)^{1/2}$ respectively [36].

VI. AUTOMATIC ANALOG CIRCUIT DESIGN OPTIMIZER

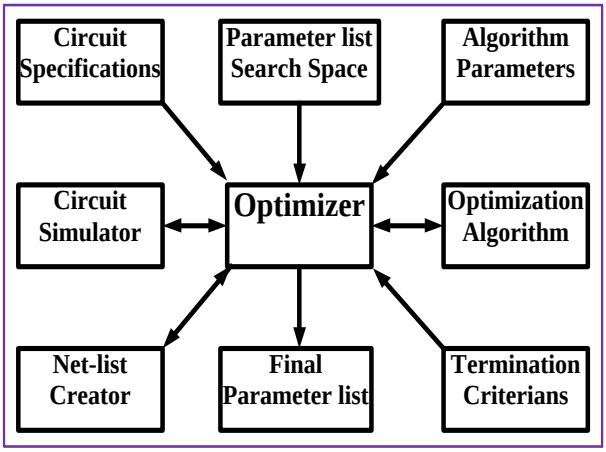

Fig. 9. block diagram of optimizer [44].

An optimizer employs the optimization technique and a circuit simulator to conceptualize a customized circuit with the desired ideal specifications. The optimizer provides synchronization between the optimization algorithm and a circuit simulator. It can generate a net-list based on the parameters optimization algorithm, and initialize the circuit simulation. It can analyze the output of the simulator to generate new sets of parameters. The conceptual block diagram of the optimizer is shown in Fig 9.

The parameters of a particular circuit are estimated using the lower and upper bounds of its design. For devices with CMOS technology, these include length and width of the numerous MOS. A particular circuit can be equipped with a set of parameters through the optimization algorithm. These are then simulated and tested against pre-defined test cases. The errors are calculated and the results of the simulation are analyzed. The calculated error then triggers the new set of parameters that the optimization algorithm will generate. The aim of the optimizer is to minimize the errors. The root mean square percentage error is given below.

$$RMS(\%)error = \sqrt{\sum_{i=1}^{N} E_i} \times 100 \qquad (10)$$

$$E_i = \begin{cases} 0 \quad if\ i^{th}\ specification\ is\ satisfied \\ \left(\dfrac{OS_i - DS_i}{DS_i}\right)^2 \quad ,otherwise \end{cases} \qquad (11)$$

Where the number of specifications is expressed as N, OS_i is the i^{th} obtained specification, and DS_i is the i^{th} specification for simulation. The optimization algorithm's objective is to ensure that the device's specifications are always equal. This can be achieved by minimizing the percentage of RMS errors that occur due to the errors.

VII. FLOW DIAGRAM OF THE AUTOMATED SIZING TECHNIQUE

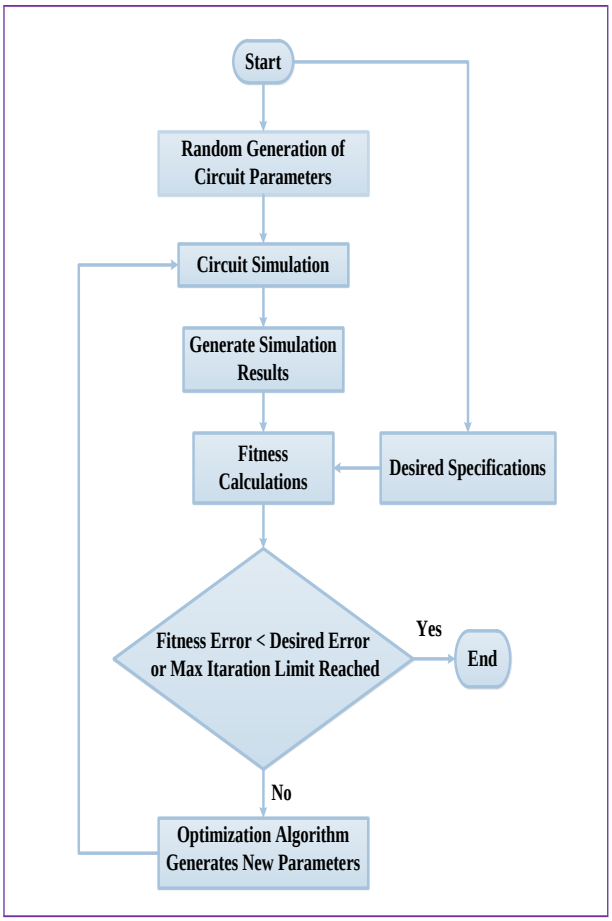

Fig. 10. Flow diagram of the automated sizing technique [45].

Fig 10 shows the flow diagram of the automated sizing technique. The automated sizing technique is primarily focused on determining the optimal width of the PMOS and NMOS transistors, and the value of the resistors, capacitors, and the bias currents of the given circuit. The PSO algorithm can be interfaced with a simulation software tool. It is implemented in C and can be used for different applications. The optimization process involves calculating the particle position vectors for the channel width of the NMOS transistor and PMOS transistor, as well as for the value of capacitor, resistor, and bias current. The error function is evaluated in every iteration of the circuit simulation. The automated procedure for circuit sizing will stop working if a termination criterion is met. The minimum error functions and maximum repetitions will be considered as the termination criteria. It is calculated according to the following equation [46].

$$F_{error} = \sqrt{\sum_{j=1}^{n}\left(\frac{Specifications_{desired} - Specifications_{simulated}}{Specifications_{desired}}\right)^2} \quad (12)$$

VIII. LITERATURE REVIEW AND PERFORMANCE IMPROVEMENT TECHNIQUES

An operational transconductance (OTA) amplifier is essential in modern electronic systems because it is used in signal-processing applications, such as biosensors and filters. Due to the increasing number of performance metrics, the availability of next-generation OTAs has become a vital component in developing new technologies. The design optimization of CMOS OTAs can help improve their performance in diverse applications. Recent research has shown that advanced algorithms can be used to enhance the parameters of the design, resulting in significant gains in power consumption, bandwidth, and gain.

The design of complex analog integrated circuits is very time-consuming and requires specialized skills. Due to the nature of the work involved, the development of automated CAD tools for designing analog circuits is not as advanced as their digital counterparts. The analytical and probing nature of the design technologies used in analog circuits makes them ideal for various applications. The design parameters of Op-amp devices are considered with the help of a two-stage Op-amp design process and a firefly algorithm. The design parameters of an operational amplifier, as Gain, Slew rate, ICMR, and CMRR are obtained using the firefly algorithm. The performance of the FA when it comes to optimizing the two-stage CMOS Opamp parameter was better than that of the earlier methods. The simulation of the two-stage Op-amp process in the CADENCE software generated a value of Gain at 77.66 dB and a Slew rate of 31.6 V/μs. The simulation results of the two-stage Op-amp process using the CADENCE VIRTUOSO software demonstrate that the design specifications for firefly-based circuits converge with those of traditional methods. They also confirm that the Firefly algorithm offers better performance when it comes to optimizing the power dissipation, Gain, and CMRR parameters [17].

The generic topology selection method on Operational Transconductance Amplifier analog electronic circuits design was demonstrated on an example using an embedded circuit sizing procedure. The paper presents a tool that can be used to design an analog circuit. It consists of a selection procedure and automatic sizing. These two steps can significantly reduce the computation time and effort involved in the design process. The automatic selection procedure for tree-based topologies only takes into account a small subset of the topologies in a given pool. The automatic optimization method then divides the various simulation-based optimization steps into sequential steps. This method eliminates the need for additional design variables and allows designers to focus on the most important performance parameters. The new approach, which is demonstrated in the OTA circuit class, involves a generic method for the automatic selection and sizing of analog circuits. It works by supporting a part-sizing procedure followed by a final sizing step. The part-sizing process is carried out in a set of simulations, which are node-specific. The resulting optimization is then performed in a simulation-based optimization. The overall simulation effort is significantly reduced compared to traditional techniques, as the process is combined with a selection loop. The system's interactive user interface makes it easier for analog designers to carry out their work. The part-sizing process and topology selection are then integrated into an analog design environment, where they can be used to improve the productivity of an analog designer [40].

The class-AB OTA can be improved by implementing a high slew rate. The component is equipped with a low quiescent current and implemented through a slew-rate boost technique. The researchers also noted that the feedback loop can address temperature, voltage, and process fluctuations caused by the enhancement transistors. Most commonly, class-AB OTA is utilized in the design of various electronic components, such as DAC, ADC, DC-DC converters, low-dropout regulators, and switch-capacitor circuits. In a study, the researchers were able to demonstrate the performance of the class AB OTA in a delta-sigma modulation system. The designed

and simulated circuit was made utilizing a 180 nm CMOS technology. Although an increase in the output bias current can boost the OTA slewing operation, it can also increase power consumption, decrease accuracy, and decrease DC gain. The slew rate is determined by comparing the maximum output current with the load capacitance. An increase in the amount of bias current can also be used to boost the slew rate of the load capacitance [43].

The folded Cascode OTA utilizes this technique to reduce its power consumption. The Folded Cascode OTA was selected due to its ability to short the output and input terminals with minimal swing restrictions. High-speed applications can benefit from the Folded Cascode OTA's ability to deliver large bandwidth and high gain. Low power consumption can significantly reduce the output of the Folded OTA. With an increase in gain, it offers a considerable reduction in power consumption. The use of self-cascode eliminates the need for high compliance voltages in output nodes. This type of structure provides a high output impedance for enhanced power gain. It can also be utilized in low-voltage applications. The stacking technique involves splitting a transistor into two. This allows the device to maintain the same gate length and width while reducing power consumption. This Folded Cascode OTA has a lower noise effect [47].

Current buffer circuits are commonly used in the design of devices to enhance their operating frequencies. An OTA current buffer-based compensate technique can be placed in the second pole frequency to replace the nulling resistor. The use of the current buffer technique and the Miller compensation method for the CMOS OTA takes advantage of the power supply ripple caused by the Miller capacitance. It provides an alternative control for operation amplifiers at high frequencies. A new design utilizing a current buffer and a pair of Miller capacitances has been presented for low-voltage devices with high frequencies. The aim of this design is to boost the device's operating frequency. The design's output resistance is large even in a small area and provides a load advantage due to the mirror topology. The design's load advantage can be used to enhance the CMRR's performance [48].

The use of a bulk-driven OTA that utilizes a feed-forward compensation method using 180 nm technology has been discussed in detail. Even though lower supply voltages lead to lower power consumption, maintaining a larger threshold voltage to minimize sub-threshold currents is required. One of the most effective techniques to address the issue of threshold voltage is by utilizing bulk-driven input MOSFETs, which are commonly used in weak inversion mode. A significant gain can be achieved by implementing an enhanced bulk-driven OTA [49].

This technique explains a high-speed and low-power complementary input folded trans-conductance amplifier for use in the parallel pipeline ADC. The OTA is an essential component of an ADC, as its power consumption and conversion rate are affected by its performance. This technique presents a parallel pipeline design that utilizes the DSSH technique for double sampling. It shares the OTA between two ADC channels. A folded cascode OTA that's equipped with regulated and fully differential gain boosting. The proper layout optimization provided a huge boost to the OTA's efficiency [50].

OTA Recycling Folded Cascode Technique offers a substantially enhanced performance compared to the conventional one. This amplifier can be utilized with old or recycled currents and devices to carry out various tasks. It offers a significantly better performance than its conventional counterpart. This amplifier utilizes previously idle devices in its signal path, which leads to slew rate, gain, and transconductance enhancements. In addition, the offset analysis and the input-referred noise performed on the suggested modifications show that they don't affect the design metrics. [51].

The presented double-recycling technique for folded Cascode OTA is an example of an improved version of the folded Cascode. It also recycles the folded cascode and improves its recycling counterparts. The computer simulations and theoretical evaluations performed on 65nm CMOS technology substantiate the proposed DRFC OTA's reasonable merits. This DRFC OTA represents another major step in enhancing the performance of the FC, IRF, and RFC variants [52].

A two-stage structure for operational transconductance is proposed, which would feature high stability, high speed, and large bandwidth. This can be achieved by utilizing a single intensifier, which would act as a cascode enhancer. A few essential parameters, like the number of channels, are also determined and analyzed hypothetically. The previously planned two-arrange intensifier has been fixed using Hspice. The related parameters such as the pickup data transmission frequency of 635 MH is acquired. The amplification level is more than a hundred dB, and the yield swing is 4V. The total transconductance of the OTA is 8.8 A/V [53].

The new family of operational amplifiers is composed of single-stage topology devices that feature non-linear current amplifiers. The suggested architecture of the VMA ensures that it doesn't require an external frequency compensator. It also has low-temperature deviations and sensitivity to temperature changes. The characteristics of the new family of OTAs are designed to meet the

requirements of low-power switched capacitors and multi-decade load-capacitance specifications. The proposed architecture of the VMA features various analytical expressions that are optimized for different regions of operation to minimize the time it takes to settle the VMA in discrete-time circuits. An example of an integrated OTA design with comprehensive simulation and evaluation results is also provided. An integrated case of an OTA design is provided with the necessary evaluation and simulation results. It is based on the 0.18micro-meter 1P6M MiM 1.8V CMOS technology. The suggested architecture is compared to the current generation of Class-AB Op-Amps and OTA literature [54].

The new hybrid mode two-stage OTA is a power-efficient inverter stacking amplifier that can achieve 6-time current reuse while maintaining a 1V supply. It can also provide the best NEF among the reported devices. The input AC coupling process can be implemented using the splitting of feedback capacitors without additional hardware costs. A simple biasing circuit based on a replica is created to ensure robust operation across different PVT variations. This OTA's prototype can be utilized for a type of action-potential recording that's capable of handling a signal bandwidth of 10 kHz to 250 Hz. The open-loop gain of the HM-OTA prototype is 76 dB. The nominal closed-loop gain is 26 dB, with CF and CS being 400 fF and 8 pF respectively. For the stack 2 & stack 3 variants, the SPICE simulation of the NEF was done at 1.26 and 1.07. The core area of the stack 2 & stack 3 devices' amplifiers is 0.01 mm2 and 0.02 mm2. Almost total areas of the closed-loop amplifier in these variants are 0.22 and 0.29 mm2, which is dominated by capacitors. It can be utilized for applications that require a high energy or power supply, such as medical devices and wireless sensors. A prototype with a 180 nm CMOS process has a noise level of 5.5μVrms and consumes only 0.25μwatt of power. The noise efficiency factor (NEF) of this hybrid mode two-stage OTA prototype at 1.07, which makes it the best power-efficient amplifier in the market. The work indicates that the NEF boundary has been pushed to a new level due to the new tradeoff among power, noise, & pushes of the NEF boundary to a new level [55].

The systematic approach is to reduce the trans conductors that are used by an OTA-capacitor filter to achieve a reduction in its active area, hardware cost, and power consumption. The suggested method combines an OTA with a linearized local feedback technique and an external trans conductance booster. The suggested OTA uses a combination of current division and source depletion to achieve low transconductance and enhance its linearity. This study Proposed, a low-voltage OTA-C filter can be used for bio-signal sensors that require a power-efficient and area-efficient operation. The suggested topology for an integrated capacitor can be used with no additional output stage and the measurement results of the prototype also indicated that it can be utilized as a 5^{th}-order ladder Butterworth OTA-C filter as an electrocardiograph signals acquisition device. The device can operate with a supply voltage of just 1 V, minimizing its power consumption by implementing an OTA circuit under a weak inversion. A prototype of an electronic device that uses a 1P6 M 180 nm CMOS technology has been fabricated to validate the suggested technique. The measurement results of the suggested device revealed that it can acquire an ECG signal with a bandwidth and dynamic range of 250 hertz and 61.2 dB. In addition, it can consume 41 nW of power. In addition, it can achieve a power consumption of approximately 41 n W, and a figure of merit of approximately 5.4 X 10^{-13}. The suggested filter has an active area of 0.24 mm^2 An electronic device can be fabricated with a high-order filter by implementing various low-order filters, such as RLC networks and multi-loop feedback topologies. [56].

The study presents the analysis and design of a recycling folded cascode with enhanced positive feedback and an improved input path. This leads to a significant increase in transconductance. The proposed circuit, which includes the CMFB and bias circuits, was evaluated using the HSPICE and TSMC 90 nm circuit simulator at 1.2 V. The results of the simulation indicated that it can achieve a power dissipation of 359 μW, 75 dB DC gain, and 357 MHz gain bandwidth. The researchers noted that their proposed circuit had a gain enhancement that was 22 dB higher than that of recycling. In addition, it had a 207 MHz GBW power output increase when compared to recycling. They performed Monte Carlo simulations to check the device's reliability and robustness against temperature, supply voltage, device dimensions, and corners. The complexity of mixed-mode and analog-only circuits in modern CMOS technology has led to more complicated OTA setups. This study provides an overview of the improved RFC and the suggested circuit improves the transconductance by providing an input path and boosting the output impedance. The researchers used HSPICE and a 90 nm CMOS process to verify the robustness. The simulations showed that its design exhibited a 75 dB DC gain and a 357 MHz GBW, which are better than FC, RFC, and PRFC. It also consumed the same amount of power which is360μW. The suggested circuit exhibited better FOMs than the existing OTAs. This shows the excellence of the design [57].

The researchers suggested OTA has a low power consumption of around 28 nW- 270 nW and a low transconductance of around 0.62nS–6.28nS. It is suitable for low-frequency biomedical sensors with interface applications. The integrated device is also equipped with a channel-length modulation effect that is utilized in a

rail-to-rail. The device has a low current-voltage linearity error of 1.5% when operating in a 1V voltage supply at a 1-Vpp asymmetrical drive. Linearity of the output current also is robust at the THD (Total Harmonic Distortion) level of 0.8 On the other hand, a 2-Vpp input drive has a THD of 0.2% and a linearity error of 0.3%..The linearity error is well-suited for the variations in the PVT (process voltage and temperature). This suggested device is fabricated using 180 nm CMOS technology. The temperature drift of the transconductance was measured at 10 pS/^{0}C. They do not consider the noise generated by an ant aliasing trans-conductor-C filter when designing the device. In a single-stage topology, the noise can be reduced by implementing the device. It should be noted, however, that the narrow driving range of a single-stage topology results in tradeoffs between preserving high-driving amplitude and maintaining low-noise levels. Various technological solutions can be utilized to address these challenges, such as low-noise CMOS technology with lower parameters of KFN and KFP. The various techniques used to realize linear LTAs include current division, current cancellation, source degeneration, and floating gates. The exact channel-length modulation impact of LTA realization on the prototype amplifier presented has not yet been fully studied. Although the design of the proposed device is interesting, it utilizes a supply voltage of 5 V. The evaluation of the proposed solution against modern circuits using the same materials was carried out to determine its performance. The results of the study were collected by a signal more than the supply voltage. The noise level in this device is relatively high, and it doesn't exhibit the same SNR as other solutions. On the positive side, it performed well in terms of its supply voltage and its low power consumption. Even though the linearity of the integrated device was maintained across different frequencies, the noise in the proposed device is still high. Temperature parameters could not be compared due to the lack of published literature about them [58].

The paper presents a method that uses the adaptive genetic algorithm known as GA to improve the CMOS operational amplifier's parameters. The optimization step can be performed in multiple objective modes, taking into account various specifications. The suggested device should be designed for various specifications; it should be considered a multi-objective optimization. With that in mind, GA is better than other optimization methods when dealing with multi-objective issues. The techniques can be applied to design various types of operational amps, like DC gain, power, noise, UGB, and phase margin. They can be performed with multiple objectives, taking into account the complexity of the design process and the device's multiple specifications. Through the use of the GA and the manual skills of an analog circuit designer, the multiple objective optimization problems related to the design can be solved. The results of the simulation revealed that the method can efficiently and accurately optimize the parameters of various analog circuits [59].

IX. CONCLUSION

This review has covered the different OTA architectures and their associated techniques to optimize their performance. In addition, the advantages and disadvantages of each architecture have been presented. The increasing complexity of the circuit during the development of an architecture leads to higher performance parameters. The lower power consumption and high gain of the Telescopic Cascode design architecture can be achieved through the degradation of the signals. On the other hand, In the Folded Cascode configuration, high gain, high swing, and high bandwidth can be achieved with the power consumption increase. The Folded Cascode design can also achieve high bandwidth, high gain, and high swing with the increase in power consumption. The reduction of power consumption is becoming an important research topic within the analog electronics sector. In battery-operated devices, low power consumption has gained important parameter that affects area, speed, and gain.

REFERENCES

[1] P. P. Prajapati and M. V Shah, “Automated sizing methodology for CMOS miller operational transconductance amplifier,” in *Soft Computing: Theories and Applications: Proceedings of SoCTA 2016, Volume 2*, 2018, pp. 301–308.

[2] G. Stehr, H. E. Graeb, and K. J. Antreich, “Analog performance space exploration by normal-boundary intersection and by Fourier–Motzkin elimination,” *IEEE Trans. Comput. Des. Integr. Circuits Syst.*, vol. 26, no. 10, pp. 1733–1748, 2007. DOI: 10.1109/TCAD.2007.895756

[3] M. G. R. Degrauwe *et al.*, “IDAC: An interactive design tool for analog CMOS circuits,” *IEEE J. Solid-State Circuits*, vol. 22, no. 6, pp. 1106–1116, 1987. DOI: 10.1109/JSSC.1987.1052861

[4] N. Lourenço and N. Horta, “GENOM-POF: multi-objective evolutionary synthesis of analog ICs with corners validation,” in *Proceedings of the 14th annual conference on Genetic and evolutionary computation*, 2012, pp. 1119–1126. https://doi.org/10.1145/2330163.2330318

[5] R. U. Ahmed, E. A. Vijaykumar, H. S. Ponakala, M. Y. V Balaji, and P. Saha, “Design of double-gate CMOS based two-stage operational transconductance amplifier using the UTBSOI transistors,” *UPB Sci. Bull., Ser C Electr Eng. Comput. Sc*, vol. 82, no. 2, pp. 173–188, 2020.

[6] S. Gaonkar, P. S. Sushma, and A. Fathima, “Design of

high CMRR two stage gate driven OTA using 0.18 µm CMOS Technology," in *2016 International Conference on Computer Communication and Informatics (ICCCI)*, 2016, pp. 1–4.

[7] G. Vasudeva and M. Jatkar, "Design of High Performance Operational Transconductance Amplifier," *ACS J. Sci. Eng.*, vol. 3, no. 2, pp. 21–30, 2023.

[8] K. Deb, A. Pratap, S. Agarwal, and T. Meyarivan, "A fast and elitist multiobjective genetic algorithm: NSGA-II," *IEEE Trans. Evol. Comput.*, vol. 6, no. 2, pp. 182–197, 2002.

[9] E. H. L. Aarts, *Simulated annealing: Theory and applications*. Reidel, 1987.

[10] E. Rashedi, H. Nezamabadi-Pour, and S. Saryazdi, "GSA: a gravitational search algorithm," *Inf. Sci. (Ny).*, vol. 179, no. 13, pp. 2232–2248, 2009.

[11] J. Kennedy and R. Eberhart, "Particle swarm optimization," *Proc. ICNN'95 - Int. Conf. Neural Networks*, vol. 4, pp. 1942–1948, doi: 10.1109/ICNN.1995.488968.

[12] M. Dorigo, "Ant colony optimization," *Scholarpedia*, vol. 2, no. 3, p. 1461, 2007.

[13] X.-S. Yang, "Firefly algorithm, stochastic test functions and design optimisation," *Int. J. bio-inspired Comput.*, vol. 2, no. 2, pp. 78–84, 2010.

[14] X.-S. Yang and S. Deb, "Cuckoo search via Lévy flights," in *2009 World congress on nature & biologically inspired computing (NaBIC)*, 2009, pp. 210–214.

[15] B. P. De, R. Kar, D. Mandal, and S. P. Ghoshal, "Soft computing-based approach for optimal design of on-chip comparator and folded-cascode op-amp using colliding bodies optimization," *Int. J. Numer. Model. Electron. Networks, Devices Fields*, vol. 29, no. 5, pp. 873–896, 2016.

[16] A. Fortes, F. A. Quirino, L. A. da Silva, and A. Girardi, "Low power bulk-driven OTA design optimization using cuckoo search algorithm," *Analog Integr. Circuits Signal Process.*, vol. 106, pp. 99–109, 2021.

[17] K. Archana, R. Kumar, S. Nath, and P. K. Srivastava, "Optimization of Two-Stage Operational Amplifier Using Firefly Algorithm Considering Environmental Constraints," *Asian J. Water, Environ. Pollut.*, vol. 19, no. 6, pp. 45–50, 2022.

[18] R. Kumar, A. Rajan, F. A. Talukdar, N. Dey, V. Santhi, and V. E. Balas, "Optimization of 5.5-GHz CMOS LNA parameters using firefly algorithm," *Neural Comput. Appl.*, vol. 28, no. 12, pp. 3765–3779, Dec. 2017, doi: 10.1007/S00521-016-2267-Y.

[19] R. Kumar, F. A. Talukdar, A. Rajan, A. Devi, and R. Raja, "Parameter optimization of 5.5 GHz low noise amplifier using multi-objective Firefly Algorithm," *Microsyst. Technol.*, vol. 26, no. 10, pp. 3289–3297, Oct. 2020, doi: 10.1007/S00542-018-4034-8.

[20] M. Panda, S. K. Patnaik, A. K. Mal, and S. Ghosh, "An evolutionary-based design methodology for performance enhancement of a folded-cascode OTA using symbiotic organisms search algorithm and gm/ID technique," *Analog Integr. Circuits Signal Process.*, vol. 105, no. 2, pp. 215–227, 2020.

[21] S. Akashe and S. Goswami, "Analysis and Design of Two-Stage Operational Transconductance Amplifier".

[22] U. Kumari and R. Yadav, "A Review About Analysis and Design Methodology of Two-Stage Operational Transconductance Amplifier (OTA)," in *Proceedings of International Conference on Data Science and Applications: ICDSA 2022, Volume 2*, 2023, pp. 849–860.

[23] S. Gaonkar and P. S. Sushma, "Modeling, design and analysis of high CMRR two stage gate driven operational transconductance amplifier using 0.18 µm CMOS technology," in *2016 3rd International Conference on Computing for Sustainable Global Development (INDIACom)*, 2016, pp. 329–334.

[24] A. Mann, M. T. Scholar, and M. DCRUST, "design of operational transconductance amplifier for application in active filters: a review".

[25] M. U. Vadodaria, R. Patel, and J. Popat, "A Review on Operational Transconductance Amplifier (OTA) Using 180nm Technology," *Int. J. Adv. Eng. Res. Dev.*, vol. 1, no. 11, pp. 215–219, 2014.

[26] A. Dendouga, S. Oussalah, D. Thienpont, and A. Lounis, "Multiobjective genetic algorithms program for the optimization of an OTA for front-end electronics," *Adv. Electr. Eng.*, vol. 2014, 2014.

[27] A. Fortes, L. A. da Silva Jr, R. Domanski, and A. Girardi, "Two-Stage OTA Sizing Optimization Using Bio-Inspired Algorithms," *J. Integr. Circuits Syst.*, vol. 14, no. 3, pp. 1–10, 2019.

[28] B. Rani and J. K. Dhanoa, "Designing of MOS Transistors in Two Stage OTA with Miller Compensation," *Int. J. Adv. Res. Electr. Electron. Instrum. Eng*, vol. 6, no. 11, pp. 8631–8637, 2017.

[29] K. B. Pandya and K. A. Shah, "Performance evaluation of different types of CMOS operational Transconductance Amplifier," *Int. J. Sci. Res.*, vol. 2, no. 3, 2013.

[30] H. Daoud, S. Ben Salem, S. Zouari, and M. Loulou, "Folded cascode OTA design for wide band applications," in *International Conference on Design and Test of Integrated Systems in Nanoscale Technology, 2006. DTIS 2006.*, 2006, pp. 437–440.

[31] H. Bouyghf, B. Benhala, and A. Raihani, "Analysis of the impact of metal thickness and geometric parameters on the quality factor-Q in integrated spiral inductors by means of artificial bee colony technique," *Int. J. Electr. Comput. Eng.*, vol. 9, no. 4, pp. 2918–2931, 2019.

[32] G. Alpaydin, S. Balkir, G. D.-I. T. on, and undefined 2003, "An evolutionary approach to automatic

synthesis of high-performance analog integrated circuits," *ieeexplore.ieee.org*, Accessed: Apr. 28, 2023. [Online]. Available: https://ieeexplore.ieee.org/abstract/document/1206446/

[33] A. Jafari, M. Zekri, S. Sadri, and A. Mallahzadeh, "Design of analog integrated circuits by using genetic algorithm," in *2010 Second International Conference on Computer Engineering and Applications*, 2010, vol. 1, pp. 578–581.

[34] I. M. Rasheed and H. J. Motlak, "Performance parameters optimization of CMOS analog signal processing circuits based on smart algorithms," *Bull. Electr. Eng. Informatics*, vol. 12, no. 1, pp. 149–157, 2023.

[35] J. Yu and Z. Mao, "Automated design method for parameters optimization of CMOS analog circuits based on adaptive genetic algorithm," in *2007 7th International Conference on ASIC*, 2007, pp. 1217–1220.

[36] B. Razavi, *Design of analog CMOS integrated circuits*. Tsinghua University Press Co., Ltd., 2005.

[37] B. Nauta, "A CMOS transconductance-C filter technique for very high frequencies," *IEEE J. Solid-State Circuits*, vol. 27, no. 2, pp. 142–153, 1992.

[38] H. Barthelemy, S. Meillere, J. Gaubert, N. Dehaese, and S. Bourdel, "OTA based on CMOS inverters and application in the design of tunable bandpass filter," *Analog Integr. Circuits Signal Process.*, vol. 57, pp. 169–178, 2008.

[39] A. B. Rahin, M. H. Ghasemi, and V. B. Rahin, "DTMOS-Based Low-Voltage and Low-Power Two-Stage OTA," 2022.

[40] A. Gerlach, J. Scheible, T. Rosahl, and F.-T. Eitrich, "A generic topology selection method for analog circuits with embedded circuit sizing demonstrated on the OTA example," in *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2017*, 2017, pp. 898–901.

[41] S. Karnik, A. K. Kushwaha, P. K. JAIN, and D. S. AJNAR, "Design of Operational Trans conductance Amplifier in 0.18 µm Technology," *Int J Mod Eng Res*, vol. 2, no. 1, 2016.

[42] A.-R. Kim, H.-R. Kim, Y.-S. Park, Y.-K. Choi, and B.-S. Kong, "Low-power class-AB CMOS OTA with high slew-rate," in *2009 International SoC Design Conference (ISOCC)*, 2009, pp. 313–316.

[43] J. Kim, S. Song, and J. Roh, "A high slew-rate enhancement class-AB operational transconductance amplifier (OTA) for switched-capacitor (SC) applications," *IEEE Access*, vol. 8, pp. 226167–226175, 2020.

[44] S. Patel and R. A. Thakker, "Automatic Circuit Design and Optimization Using Modified PSO Algorithm.," *J. Eng. Sci. Technol. Rev.*, vol. 9, no. 1, 2016.

[45] P. P. Prajapati and M. V Shah, "Two stage CMOS operational amplifier design using particle swarm optimization algorithm," in *2015 IEEE UP Section Conference on Electrical Computer and Electronics (UPCON)*, 2015, pp. 1–5.

[46] R. A. Thakker, M. S. Baghini, and M. B. Patil, "Low-power low-voltage analog circuit design using hierarchical particle swarm optimization," in *2009 22nd international conference on VLSI design*, 2009, pp. 427–432.

[47] S. Kundra, P. Soni, and A. Kundra, "Low power folded cascode OTA," *Int. J. VLSI Des. Commun. Syst.*, vol. 3, no. 1, p. 127, 2012.

[48] V. K. Bhardwaj, H. Kumar, P. Kumar, and A. Ahmed, "A low power 2 GHz unity gain frequency with 154 PSRR CMOS OTA," in *2012 International Conference on Solid-State and Integrated Circuit (ICSIC 2012) IPCSIT*, 2012, vol. 32.

[49] S. Rekha and T. Laxminidhi, "A low power, fully differential bulk driven OTA in 180 nm CMOS Technology," *Int. J. Comput. Electr. Eng.*, vol. 4, no. 3, p. 396, 2012.

[50] M. K. Hati and T. K. Bhattacharyya, "Design of a low power, high speed complementary input folded regulated cascode OTA for a parallel pipeline ADC," in *2011 IEEE Computer Society Annual Symposium on VLSI*, 2011, pp. 114–119.

[51] R. S. Assaad and J. Silva-Martinez, "The recycling folded cascode: A general enhancement of the folded cascode amplifier," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2535–2542, 2009.

[52] Z. Yan, P.-I. Mak, and R. P. Martins, "Double recycling technique for folded-cascode OTA," *Analog Integr. Circuits Signal Process.*, vol. 71, pp. 137–141, 2012.

[53] F. Jin, X. Fu, P. Niu, G. Yang, and T. Gao, "The Research of Operational Transconductance Amplifier," in *2011 International Conference on Control, Automation and Systems Engineering (CASE)*, 2011, pp. 1–4.

[54] S. Sutula, M. Dei, L. Terés, and F. Serra-Graells, "Variable-mirror amplifier: A new family of process-independent class-AB single-stage OTAs for low-power SC circuits," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 63, no. 8, pp. 1101–1110, 2016.

[55] L. Shen, N. Lu, and N. Sun, "A 1-V 0.25-$\mu\text{W} $ inverter stacking amplifier with 1.07 noise efficiency factor," *IEEE J. Solid-State Circuits*, vol. 53, no. 3, pp. 896–905, 2018.

[56] S.-Y. Lee, C.-P. Wang, and Y.-S. Chu, "Low-voltage OTA–C filter with an area-and power-efficient OTA for biosignal sensor applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 1, pp. 56–67, 2018.

[57] T. Aghaee, S. Biabanifard, and A. Golmakani, "Gain boosting of recycling folded cascode OTA using positive feedback and introducing new input path,"

Analog Integr. Circuits Signal Process., vol. 90, pp. 237–246, 2017.

[58] J. Jakusz, W. Jendernalik, G. Blakiewicz, M. Kłosowski, and S. Szczepański, "A 1-nS 1-V Sub-1-µW Linear CMOS OTA with Rail-to-Rail Input for Hz-Band Sensory Interfaces," *Sensors*, vol. 20, no. 11, p. 3303, 2020.

[59] J. Yu and Z. Mao, "A design method in CMOS operational amplifier optimization based on adaptive genetic algorithm," *WSEAS Trans. Circuits Syst.*, vol. 8, no. 7, pp. 548–558, 2009.

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